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# Road vehicles — Media Oriented Systems Transport (MOST) —

## Part 13: 50-Mbit/s balanced media physical layer conformance test plan

*Véhicules routiers — Système de transport axé sur les médias —*

*Partie 13: Plan d'essais de conformité de la couche physique en milieu équilibré à 50-Mbit/s*

Reference number
ISO 21806-13:2021(E)

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# Foreword

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The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular, the different approval criteria needed for the different types of ISO documents should be noted. This document was drafted in accordance with the editorial rules of the ISO/IEC Directives, Part 2 (see www .org/directives).

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For an explanation of the voluntary nature of standards, the meaning of ISO specific terms and expressions related to conformity assessment, as well as information about ISO's adherence to the World Trade Organization (WTO) principles in the Technical Barriers to Trade (TBT), see www .org/iso/foreword.html.

This document was prepared by Technical Committee ISO/TC 22, *Road vehicles*, Subcommittee SC 31, *Data communication*.

A list of all parts in the ISO 21806 series can be found on the ISO website.

Any feedback or questions on this document should be directed to the user's national standards body. A complete listing of these bodies can be found at www .org/members.html.

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# Introduction

The Media Oriented Systems Transport (MOST) communication technology was initially developed at the end of the 1990s in order to support complex audio applications in cars. The MOST Cooperation was founded in 1998 with the goal to develop and enable the technology for the automotive industry. Today, MOST[1)] enables the transport of high Quality of Service (QoS) audio and video together with packet data and real-time control to support modern automotive multimedia and similar applications. MOST is a function-oriented communication technology to network a variety of multimedia devices comprising one or more MOST nodes.

Figure 1 shows a MOST network example.

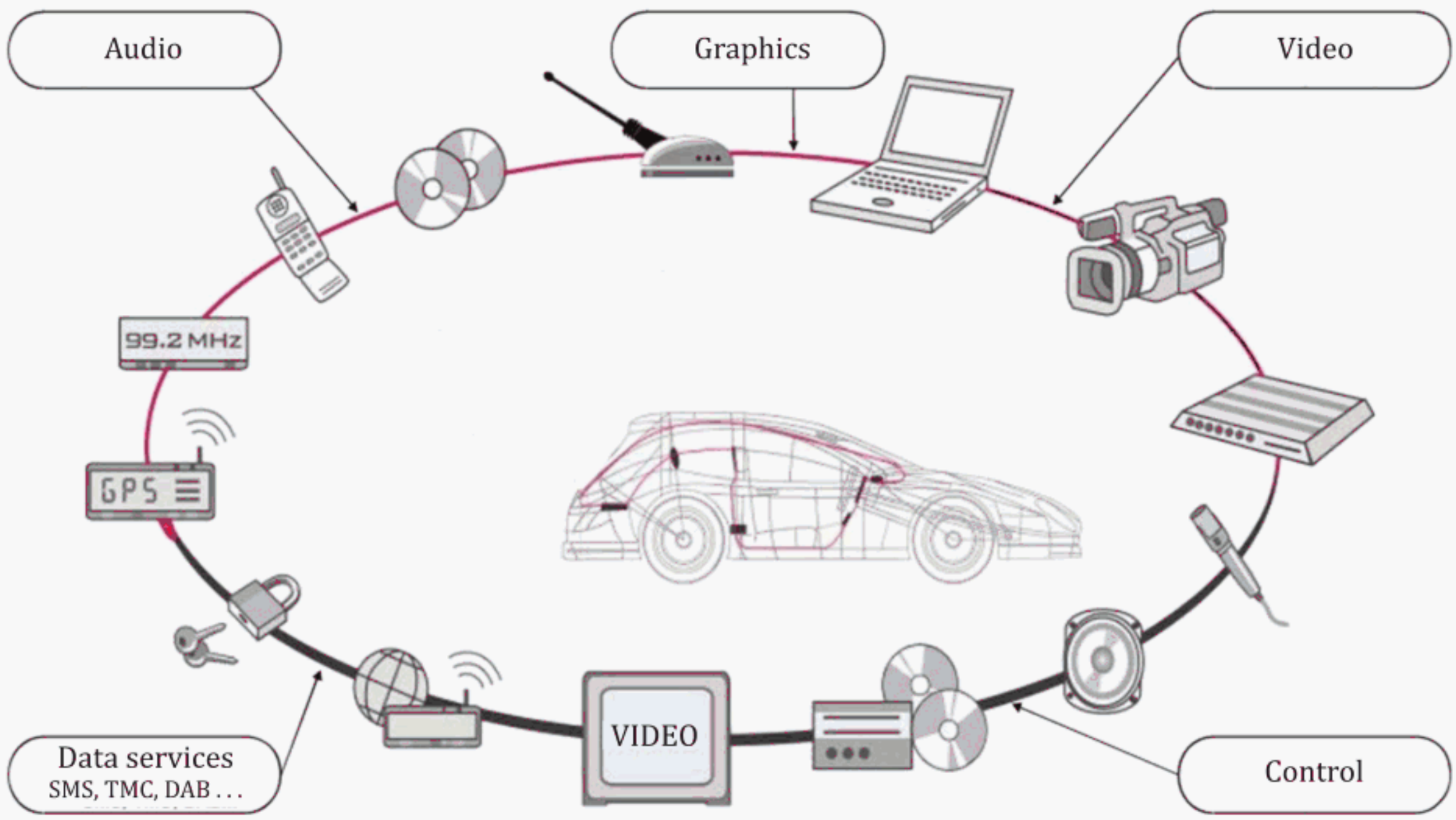


**Figure 1 — MOST network example**

The MOST communication technology provides:

— synchronous and isochronous streaming,

— small overhead for administrative communication control,

— a functional and hierarchical system model,

— API standardization through a function block (FBlock) framework,

— free partitioning of functionality to real devices,

— service discovery and notification, and

— flexibly scalable automotive-ready Ethernet communication according to ISO/IEC/IEEE 8802-3[2].

MOST is a synchronous time-division-multiplexing (TDM) network that transports different data types on separate channels at low latency. MOST supports different bit rates and physical layers. The network clock is provided with a continuous data signal.

1) MOST® is the registered trademark of Microchip Technology Inc. This information is given for the convenience of users of this document and does not constitute an endorsement by ISO.


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Within the synchronous base data signal, the content of multiple streaming connections and control data is transported. For streaming data connections, bandwidth is reserved to avoid interruptions, collisions, or delays in the transport of the data stream.

MOST specifies mechanisms for sending anisochronous, packet-based data in addition to control data and streaming data. The transmission of packet-based data is separated from the transmission of control data and streaming data. None of them interfere with each other.

A MOST network consists of devices that are connected to one common control channel and packet channel.

In summary, MOST is a network that has mechanisms to transport the various signals and data streams that occur in multimedia and infotainment systems.

The ISO standards maintenance portal (https://standards .org/iso/) provides references to MOST specifications implemented in today's road vehicles because easy access via hyperlinks to these specifications is necessary. It references documents that are normative or informative for the MOST versions 4V0, 3V1, 3V0, and 2V5.

The ISO 21806 series has been established in order to specify requirements and recommendations for implementing the MOST communication technology into multimedia devices and to provide conformance test plans for implementing related test tools and test procedures.

To achieve this, the ISO 21806 series is based on the open systems interconnection (OSI) basic reference model in accordance with ISO/IEC 7498-1[1] and ISO/IEC 10731[3], which structures communication systems into seven layers as shown in Figure 2. Stream transmission applications use a direct stream data interface (transparent) to the data link layer.

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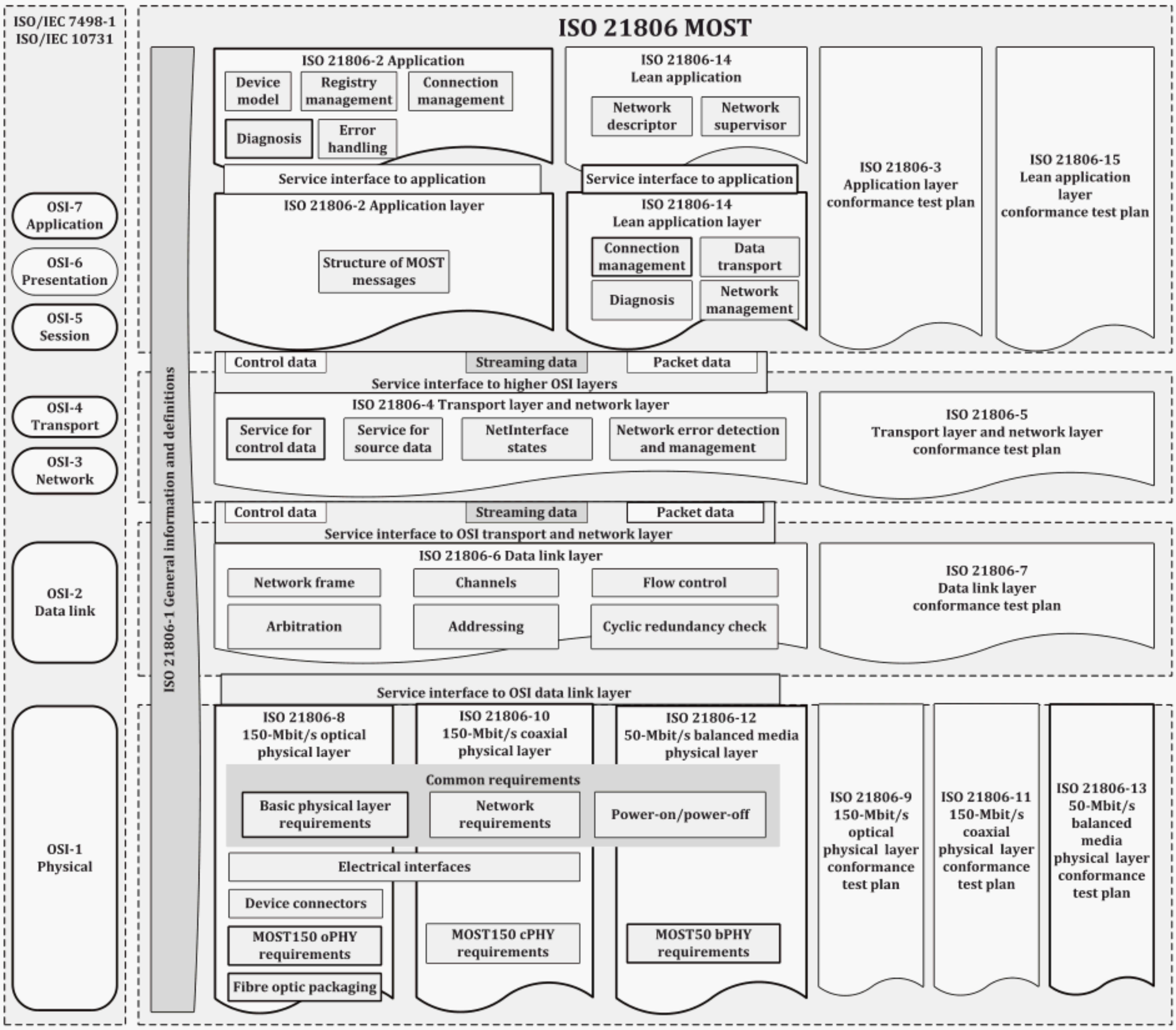


**Figure 2 — The ISO 21806 series reference according to the OSI model**

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# Road vehicles — Media Oriented Systems Transport (MOST) —

Part 13:
# 50-Mbit/s balanced media physical layer conformance test plan

## 1 Scope

This document specifies the conformance test plan for the 50-Mbit/s balanced media physical layer for MOST (MOST50 bPHY), a synchronous time-division-multiplexing network.

This document specifies the basic conformance test measurement methods, relevant for verifying compatibility of networks, nodes, and MOST components with the requirements specified in ISO 21806-12.

## 2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO 21806-1, *Road vehicles — Media Oriented Systems Transport (MOST) — Part 1: General information and definitions*

ISO 21806-12, *Road vehicles — Media Oriented Systems Transport (MOST) — Part 12: 50-Mbit/s balanced media physical layer*

EN 50289-1-8, *Communication cables — Specifications for lest methods — Part 1-8: Electrical test methods — Attenuation*

EN 50289-1-11, *Communication cables — Specifications for lest methods — Part 1-11: Electrical test methods — Characteristic impedance, input impedance, return loss*

No JEDEC JESD8C.01,[2)] *interface Standard for Nominal 3 V/3.3 V Supply Digital Integrated Circuits*

## 3 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO 21806-1, ISO 21806-12 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

— ISO Online browsing platform: available at https://www .org/obp

— IEC Electropedia: available at http://www.electropedia.org/

2) Available at https://www.jedec.org/.

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**3.1**
**intersymbol interference**
disturbance due to the overflowing into the signal element representing a wanted digit of signal elements representing preceding or following digits

[SOURCE: IEC Electropedia, 702-08-33]

# 4 Symbols and abbreviated terms

## 4.1 Symbols

| | |
|---|---|
| --- | empty table cell or feature undefined |
| $\varepsilon_r$ | relative permittivity |
| $F$ | frequency |
| $\rho_{BR}$ | bit rate |
| $\rho_{Fs}$ | network frame rate |
| $t$ | time |
| $T$ | temperature |
| $T_A$ | ambient temperature |
| $T_{Typ}$ | typical temperature |

## 4.2 Abbreviated terms

| | |
|---|---|
| AFE | analogue frontend |
| AJ | alignment jitter |
| BALUN | balanced-unbalanced |
| BEC | balanced media to electrical converter |
| BR | bitrate |
| BTR | balanced media transceiver |
| BW | bandwidth |
| Cfg | configuration |
| CH | channel |
| DC | direct current |
| DSO | digital sampling oscilloscope |
| EBC | electrical to balanced media converter |
| FFT | fast Fourier transformation |
| IUT | implementation under test |


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| | |
|---|---|
| MNC | MOST network controller |
| PG | pattern generator |
| PLL | phase lock loop |
| PSD | power spectral density |
| RBW | resolution bandwidth |
| RMS | root mean square |
| SP | specification point |
| TDR | time-domain reflectometer |
| TJ | transferred jitter |
| UI | unit interval |
| VNA | vector network analyser |

# 5 Conventions

This document is based on OSI service conventions as specified in ISO/IEC 10731[3].

# 6 Operating conditions and measurement tools, requested accuracy

## 6.1 Operating conditions

Temperature range for MOST components: $T_A$ = -40 °C to +105 °C according to ISO 21806-12:2021, 11.3.

Voltage range for MOST components: $V_{CCCN}$ and $V_{CCSW}$, with an operating range of 3,3 V ± 0,165 V according to ISO 21806-12:2021, Clause 10.

NOTE There are functional requirements for the EBC within an extended voltage supply range according to ISO 21806-12.

## 6.2 Apparatus — Measurement tools, requested accuracy

Apart from the measurement tools listed in this subclause, depending on the chosen test method and method to generate stimuli for the test, further equipment is necessary (e.g. electrical attenuator, discrete filter module to emulate cable transfer function). Performance requirements of such equipment depend on the use case.

The following list provides the measurement tools.

### 6.2.1 Oscilloscope

— digital sampling oscilloscope;

— sampling rate ≥5 gigasample/s;

— bandwidth ≥1 GHz;

— sampling memory ≥10 megasample;

— active probe (single-ended, differential).

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#### 6.2.2 VNA or TDR (TDR bandwidth ≥3,5 GHz).

#### 6.2.3 Ampere meter

— accuracy ≤2 μA;

— trigger input (for timing measurements).

#### 6.2.4 Pattern generator for generating MOST50 bPHY stress pattern

— bandwidth 100 Mbit/s;

— trigger output (for timing measurements).

## 7 Electrical characteristics

LVTTL testing of MOST devices or MOST components shall be performed according to JEDEC No. JESD8C.01.

## 8 Balanced media characteristics

### 8.1 Threshold for detection of alignment and transferred jitter

All jitter measurements are based on detection of edges in the data stream. The threshold for detecting edges is set to 0 V of the differential signal (zero-crossing). DC offset in the measurements shall be minimized as it may indirectly compromise timing-parameter results, see 10.2 and 10.3.

### 8.2 RMS signal amplitude

In ISO 21806-12:2021, 9.2, output signal power boundaries for SP2 and minimum input signal power at SP3 are defined as RMS voltage.

A waveform, signal voltage over time, is acquired on an oscilloscope. The RMS voltage $V_{\mathrm{RMS}}$ is calculated according to Formula (1).

$$V_{\mathrm{RMS}} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} V(i)^2} \tag{1}$$

where

$V_{\mathrm{RMS}}$ is the root-mean-square signal voltage;

$N$ is the number of time steps with equidistant time interval;

$V$ is the voltage amplitude at a specific time step;

$i$ is the index of summation.

RMS signal voltage amplitude gives a representation of the average signal power $P_{\mathrm{av}}$ as specified in Formula (2).

$$P_{\mathrm{av}} = \frac{V_{\mathrm{RMS}}^2}{R} \tag{2}$$

where


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$P_{av}$ is the average signal power in [W];

$V_{RMS}$ is the root-mean-square signal voltage.

$R$ resistance of 100 Ω.

In order to get to a representative average value, it requires a long-term observation. Depending on the chosen SP2 and applied channel losses, intersymbol interference impact affects the signal to be measured. It may lead to locally distributed RMS minima and maxima when choosing only short snippets of the signal. The acquired waveform shall have a minimum length of 125 µs (125 µs equals six frames with a frame rate of 48 kHz).

DC offset in the measurements shall be minimized as it may indirectly compromise RMS signal voltage amplitude results, see 10.2 and 10.3.

## 8.3 PSD of SP2 output signal

PSD as specified in ISO 21806-12:2021, 9.2 is used as a link quality criterion at SP2. The main purpose is to limit pulse shape variations and inherently limit the transmitted signal bandwidth.

Several measurement options are available to perform spectral signal analysis. A method using time-domain data acquisition followed by FFT post-processing is given for reference. Other measurement methods are permitted. In the case of discrepancies, the reference method shall be used.

PSD shall be measured with an RMS detector and using an effective RBW of 500 kHz. Besides directly measuring PSD with 500 kHz resolution bandwidth, this can be achieved by using lower RBW setting and averaging spectral results in the amount $n$ of overlapping groups of the lower RBW bands to produce the effect of 500 kHz RBW sliding window (linear scale), (i.e. measurement with RBW 10 kHz, averaged in overlapping groups of fifty bands, therefore $n$ = 50). To achieve statistical representation, the spectral density results of multiple trace segments are averaged to form the final result. The number of trace segments contributing to the averaged spectrum equals the sweep time.

The following is an example procedure for measuring PSD.

— The IUT transmitter sends multiple MOST50 bPHY PSD patterns.

— Differential signal at terminated SP2 is measured with a differential probe. Other methods to measure a single ended representation of the differential signal are acceptable (e.g. use BALUN or use test fixture with matched length 50 Ω coaxial cables, measured with 2 channels and mathematical combination).

— An oscilloscope acquires the SP2 signal. To reduce noise in the measurement channel, it is recommended to use an averaging technique for time domain data acquisition. Selecting oscilloscope sampling rate and acquisition length leads to the inherent RBW for the acquisition, which is the reciprocal of the acquired duration time. The appropriate duration can be achieved by adjusting horizontal oscilloscope settings accordingly or by acquiring longer traces and slice the trace into appropriate trace segments for the further processing.

— For further post-processing, FFT algorithm can be applied on the oscilloscope or via processing per external script on a PC. In frequency domain, PSD is then formed as a moving average (linear scale) of $n$ consecutive samples of the inherent RBW bands.

— To achieve statistical representation, the spectral density results of multiple trace segments are averaged to form the final result. The number of trace segments contributing to the averaged spectrum equals the sweep time.

— Described procedure provides spectral density for consecutive 500 kHz bands in the relevant frequency range and can be directly compared with the limit lines.

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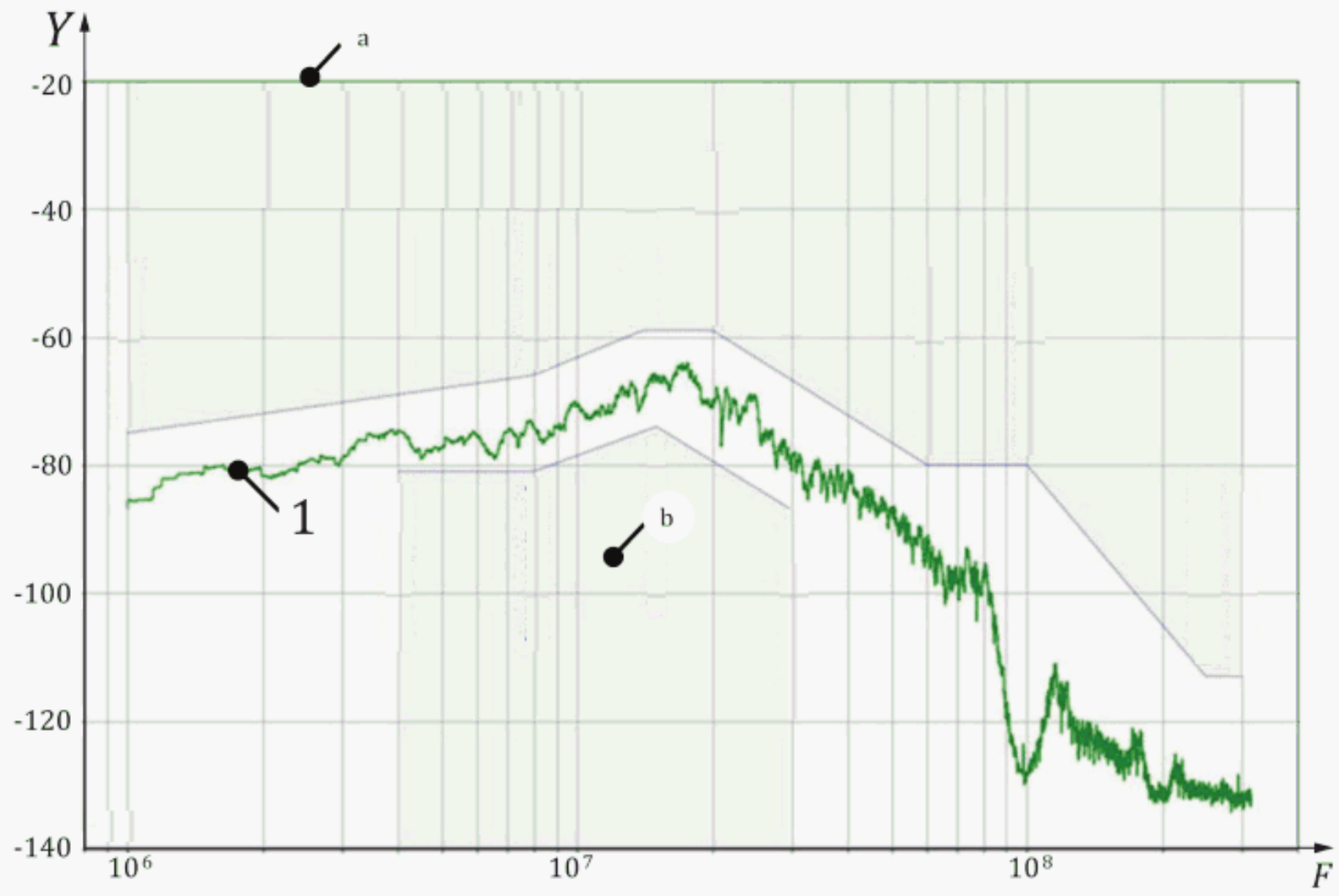
Configuration for a measurement example:

— acquisition length of 1 megasample with sampling rate 10 GHz results in a duration of 100 µs or inherent RBW of 10 kHz,

— this results in an overlap of $n$ = 50 inherent RBW bands to form effective RBW of 500 kHz,

— 100 iterations lead to a sweep time of 10 ms.

Figure 3 shows the example measurement for PSD.




**Key**

$Y$ PSD [dBm/Hz]

$F$ frequency [Hz]

1 example PSD

[a] This is the upper limit of the PSD mask.

[b] This is the lower limit of the PSD mask.

**Figure 3 — Example measurement for PSD**

PSD analysis may also be performed with a spectral analyser. The number of data points can also be lower and not produce gapless data in the specified frequency range. Settings are applied that fit the above described processing.

Figure 4 shows the test set-up for measuring PSD with an oscilloscope.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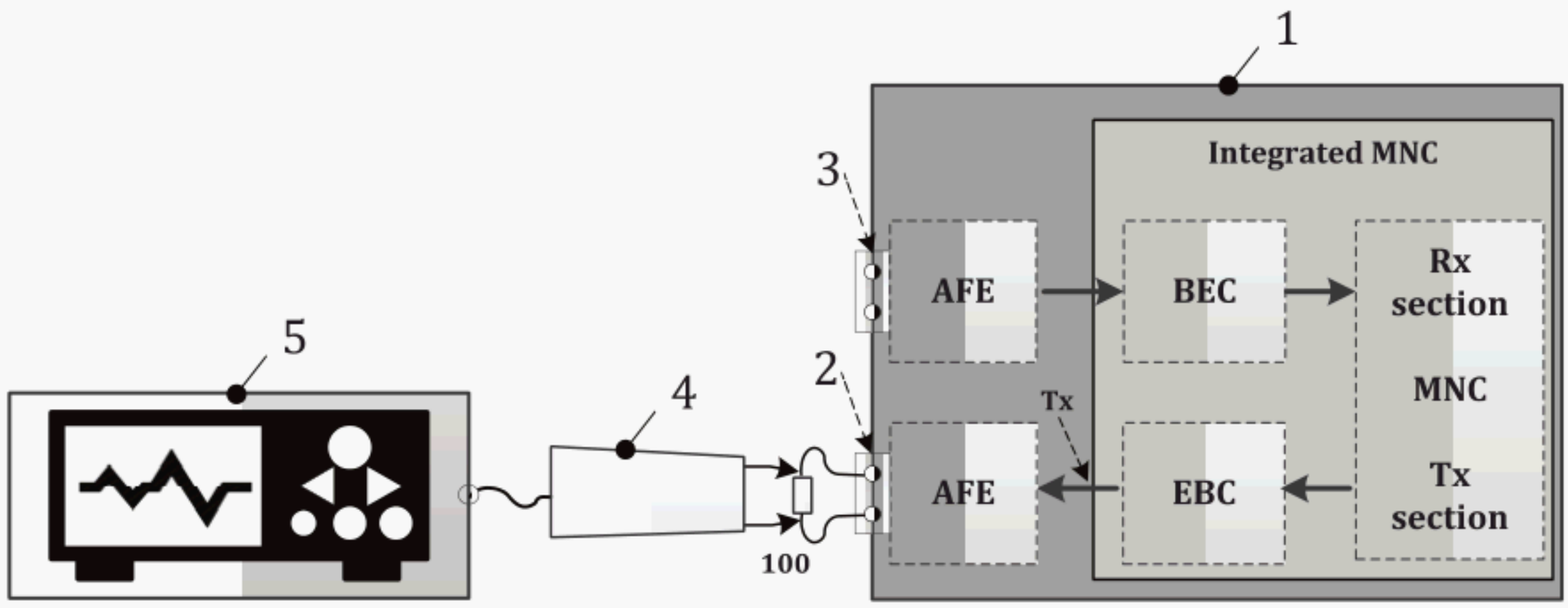


**Key**

1 MOST device
2 SP2
3 SP3
4 differential probe
5 oscilloscope

**Figure 4 — Test set-up for measuring PSD with an oscilloscope**

## 8.4 Attenuation of electrical interconnect

### 8.4.1 General

MOST50 bPHY limits the maximum attenuation for an electrical interconnect, formed of one or more cable pieces and the associated couplers and harness connectors. The maximum total length of the interconnect is 15 m. The attenuation of such an interconnect is frequency-dependent. ISO 21806-12:2021, 9.3 specifies the maximum tolerable attenuation with a limit line in the frequency range of 1 MHz to 66 MHz.

Figure 5 shows the test set-up for measuring attenuation of an electrical interconnect.

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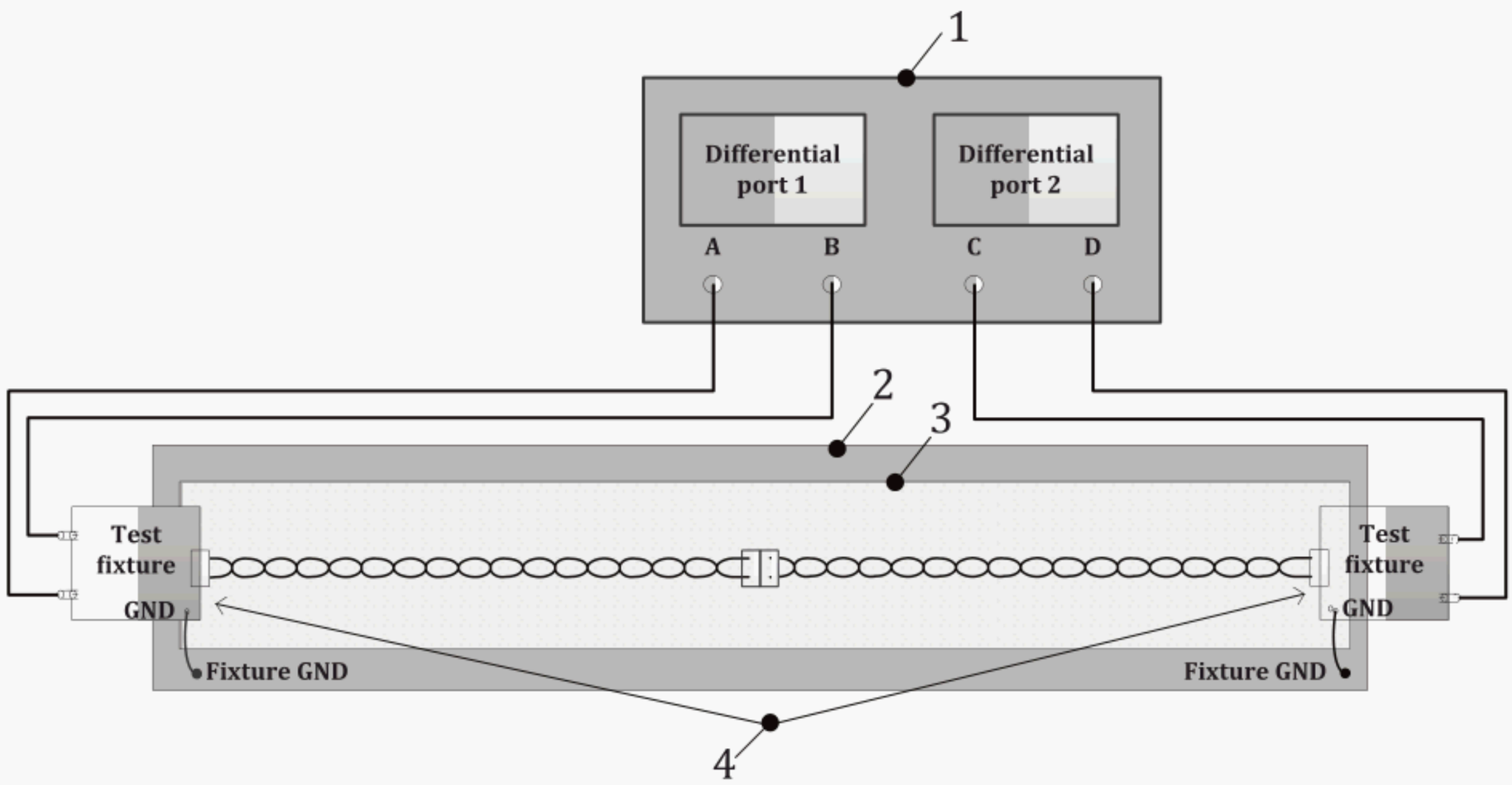


**Key**

1 VNA

2 metal plane (GND reference)

3 isolation layer

4 interconnect under test

**Figure 5 — Test set-up for measuring attenuation of an electrical interconnect**

### 8.4.2 Test procedure general

The evaluation of cable attenuation shall follow the principle as specified in EN 50289-1-8. This is performed with a network analyser, using a 4-port arrangement.

### 8.4.3 Example set-up test procedure

A test fixture is being used to connect the differential cable system to the single ended measurement equipment. For details see Annex C. The status of Annex C is informative.

When acquiring a complete set of the mixed mode scatter parameters (S-parameters) for an interconnect under test, extract the magnitude of the transfer characteristic from differential port 1 to port 2 and vice versa (differential insertion loss: SDD21 and SDD12) in dB-scale.

NOTE The cable attenuation varies with environmental conditions (e.g. temperature) and also depends on production process, properties of used materials and stability of geometric properties. It also depends on the way the interconnect under test is being arranged for the test.

The cable under test shall be placed on an arrangement with metal plane (GND-reference) at the bottom and an isolation layer (thickness 10 mm, $\varepsilon_r \leq 1{,}4$) on top. The cable shall be placed on top of the isolation layer, the cable shall be laid out with a minimum distance of 30 mm between the cable portions (either meander shaped on a flat plane or cable assembled on a conductive drum with a minimum distance to each winding). GND of test fixture shall be connected to the metal plane.

### 8.4.4 Test procedure for data acquisition

Figure 6 shows the example measurement of attenuation of an electrical interconnect.


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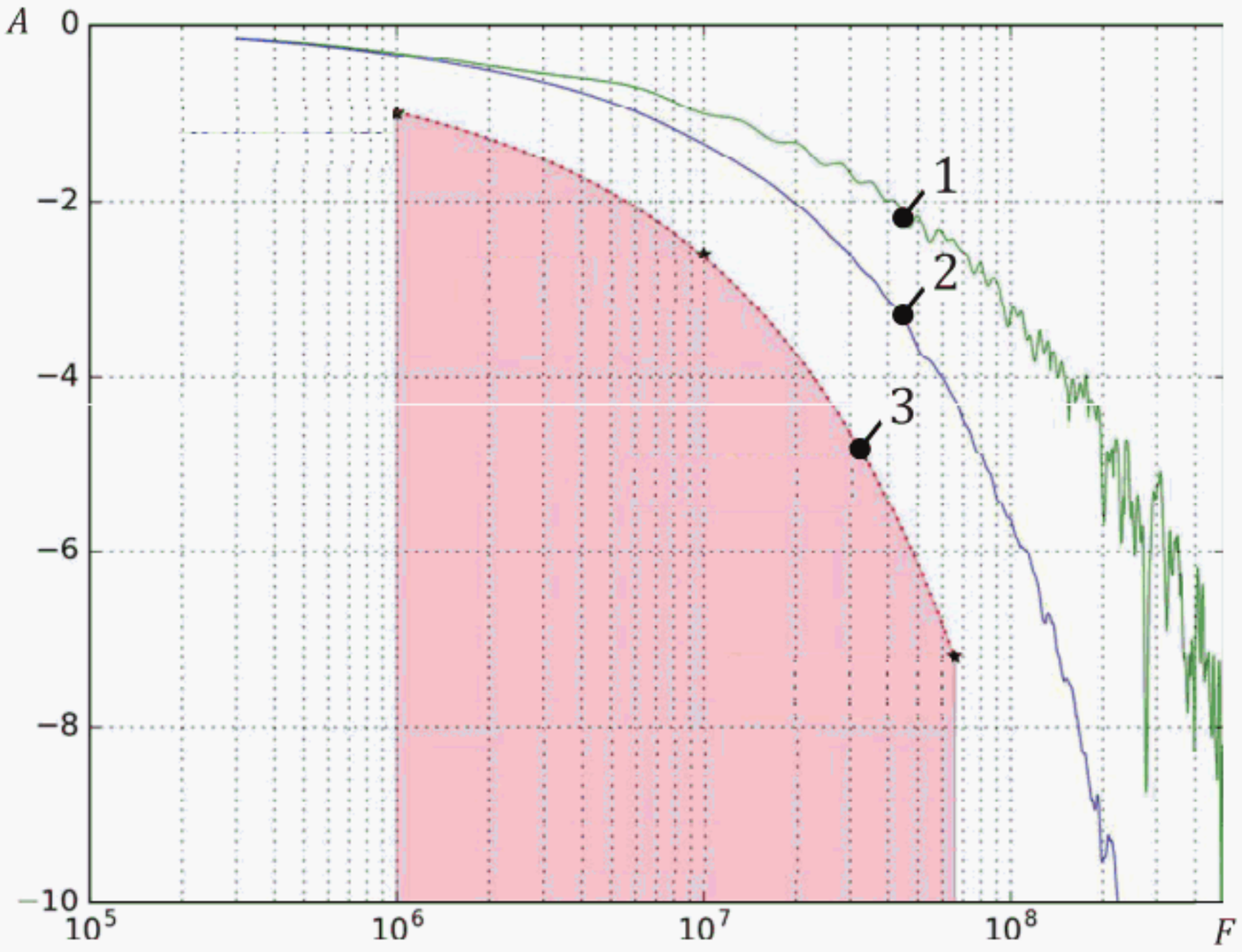


**Key**

*A* attenuation [dB]

*F* frequency [Hz]

1 example 1

2 example 2

3 attenuation limit

**Figure 6 — Example measurement of attenuation of an electrical interconnect**

### 8.4.5 Impact of attenuation on the data signal

The attenuation characteristic of electrical interconnect follows a function of frequency. Therefore, the spectrum of a data signal being fed into such channel shall be attenuated in a non-uniform manner. Attenuation affects high frequencies more than low frequencies. In consequence, transition times decrease. Shorter pulses of the signal might not achieve full amplitude swing anymore. The effect is called intersymbol interference.

The graph in Figure 7 gives an example: the SP2 signal starts with a nearly uniform amplitude on all pulses. A small intersymbol interference effect is already visible, which is caused by AFE band-filtering. The SP3 signal shows the resulting signal shape after having passed a typical electrical interconnect. Additional intersymbol interference is visible.

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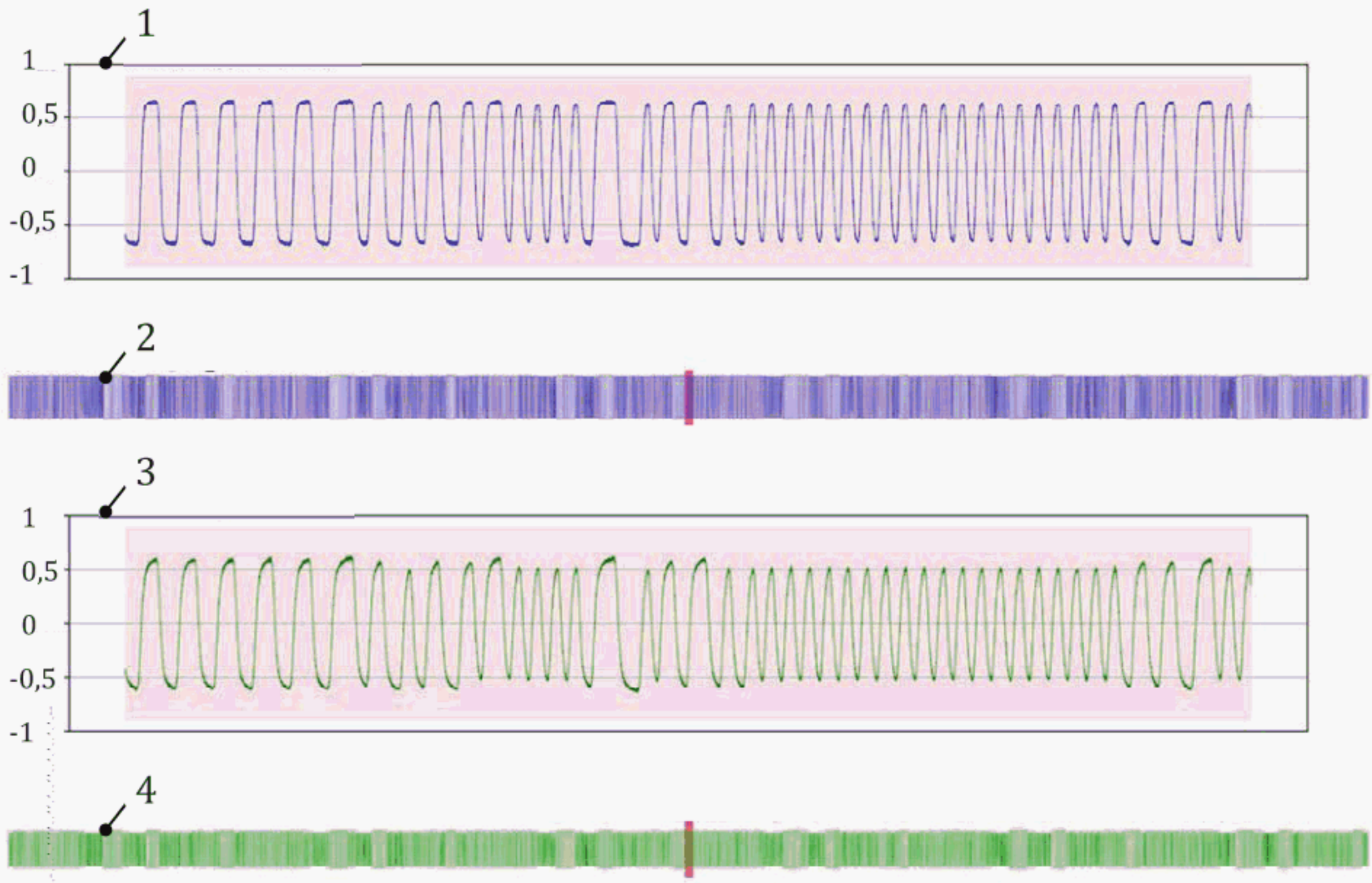


**Key**

1 zoom of typical SP2 trace

2 typical SP2 trace – signal voltage amplitude $V_{RMS}$ with the value of 545 mV

3 zoom of typical SP3 trace

4 typical SP3 trace – signal voltage amplitude $V_{RMS}$ with the value of 437 mV

**Figure 7 — Example measurement of impact of attenuation on data signal**

## 8.5 Characteristic impedance of balanced media

Characteristic impedance of balanced media shall be determined using time domain reflectometer and analysing the space-resolved wave resistance. Alternatively, frequency domain measurement results can be taken and adequately transferred into time domain.

The minimum requirement to adequately evaluate the cable impedance in the context of the specified application is given by the rise time of the time-domain reflectometry signal; it shall be <1 ns. This considers a rise time that equals 0,35 divided by the maximum signal frequency, while the maximum signal frequency is assumed with 3 times the UI rate (3$^{rd}$ harmonic). It is recommended to use a TDR with at least 3,5 GHz bandwidth, which corresponds to a rise time of a maximum of 100 ps, and post-filtering to adjust for MOST50 bPHY bandwidth requirements.

The TDR shall have two channels (CH1, CH2). The two channels shall be adjusted differentially. The near end of the electrical interconnect under test is connected to the TDR. The two wires of the pair shall be connected to the differential input of the measuring instrument. The two connection cables shall have the same high-frequency characteristics and should match with respect to length, phase velocity and attenuation. At the connection level, the ground potentials of the two lines shall be connected to one another. The far end of the interconnect under test can remain open.


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The TDR presents the result either as a differential impedance profile or as two single ended impedance profiles. For two profiles, the differential impedance of the pair is the sum of the two individual impedances as specified in Formula (3).

$$Z_{0\text{cable}} = Z_{\text{TDR_CH1}} + Z_{\text{TDR_CH2}} \tag{3}$$

where

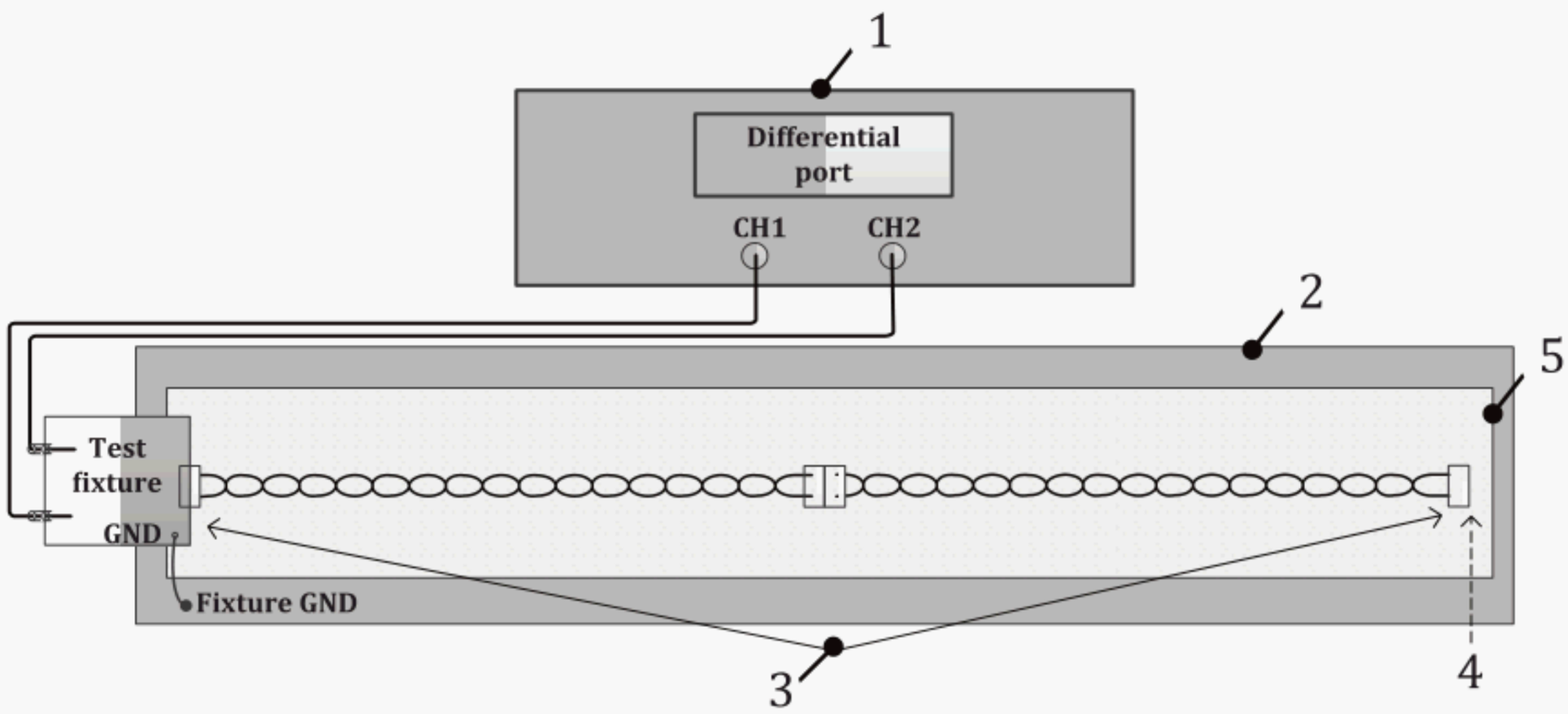
$Z_{0\text{cable}}$ is the characteristic impedance of the cable;

$Z_{\text{TDR_CH1}}$ is the characteristic impedance of the TDR channel 1;

$Z_{\text{TDR_CH2}}$ is the characteristic impedance of the TDR channel 2.

ISO 21806-12 does not define explicit requirements for impedance matching of connector and coupler components. Therefore, it is permitted to gate out area around the connector components. The interconnect under test shall be evaluated from both ends.

Figure 8 shows the test set-up for measuring characteristic impedance of balanced media, stimulating the left end of the IUT.




**Key**

1 TDR

2 metal plane (GND reference)

3 interconnect under test

4 IUT with open end

5 isolation layer

**Figure 8 — Test set-up for measuring characteristic impedance of balanced media, stimulating left end of IUT**

Figure 9 shows the test set-up for measuring characteristic impedance of balanced media, stimulating the right end of the IUT.

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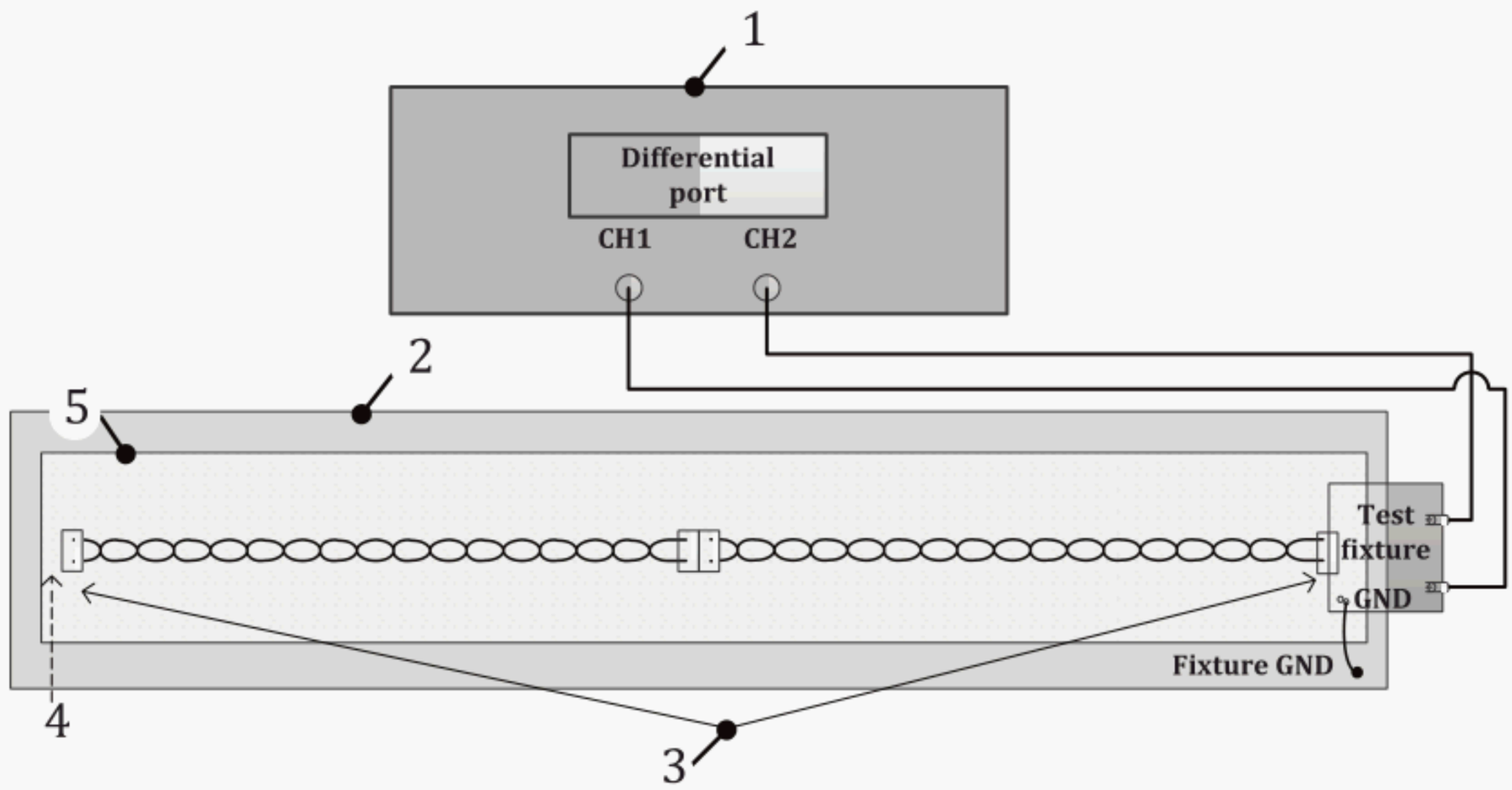


**Key**

1 TDR
2 metal plane (GND reference)
3 interconnect under test
4 IUT with open end
5 isolation layer

**Figure 9 — Test set-up for measuring characteristic impedance of balanced media, stimulating right end of IUT**

Figure 10 shows the example measurement for characteristic impedance of balanced media.


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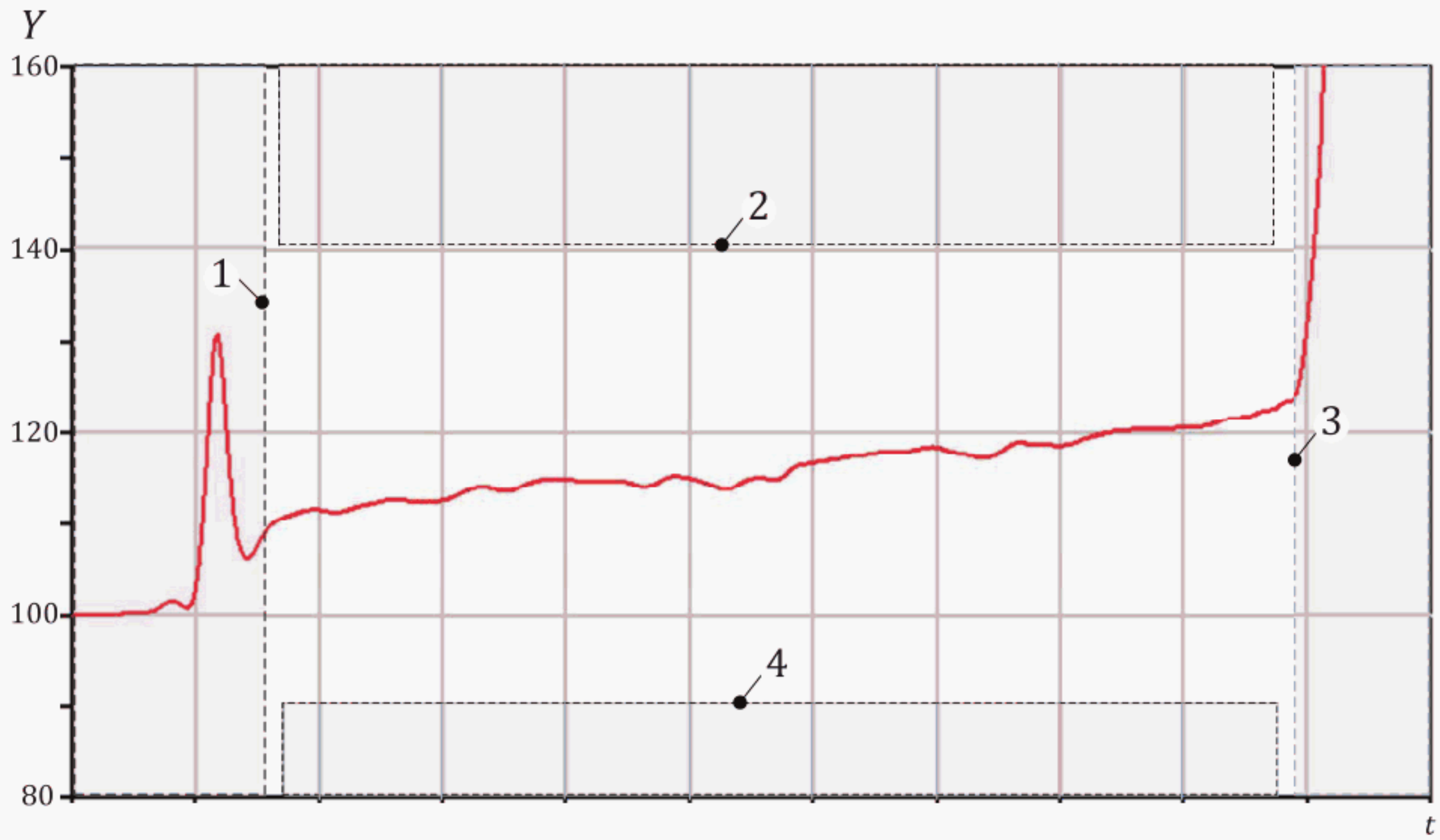


**Key**

| | |
|---|---|
| $t$ | time |
| $Y$ | characteristic impedance |
| 1 | test fixture and connector |
| 2 | upper boundary |
| 3 | open end |
| 4 | lower boundary |

**Figure 10 — Example measurement for characteristic impedance of balanced media**

## 8.6 RL of PCB interfaces

Signals going to or coming from balanced media interconnect are electrically connected on the PCB and finally end at the transceivers. The combination of board traces, passive components and board connector is summarized under the term analogue front-end (AFE). This portion of the link should closely match the characteristic line impedance. Deviations in impedance matching cause reflections; RL is the ratio between transmitted and the reflected signal energy.

ISO 21806-12:2021, 9.3 specifies a limit line in the frequency domain; the measurement, however, can be done in time – or frequency domain. The measurement set-up is a differential single port configuration, emitting a signal into the PCB interface under test (SP2 and SP3) and measuring the reflected energy.

The result shall be transferred to magnitude in dB scale and compared with the limit line.

A test fixture is being used to connect the differential cable system to the single ended measurement equipment. For details see Annex C.

A precondition is that the ECU is configured for a test mode according to Table 1, which specifies the conditions for RL measurement of PCB interfaces.

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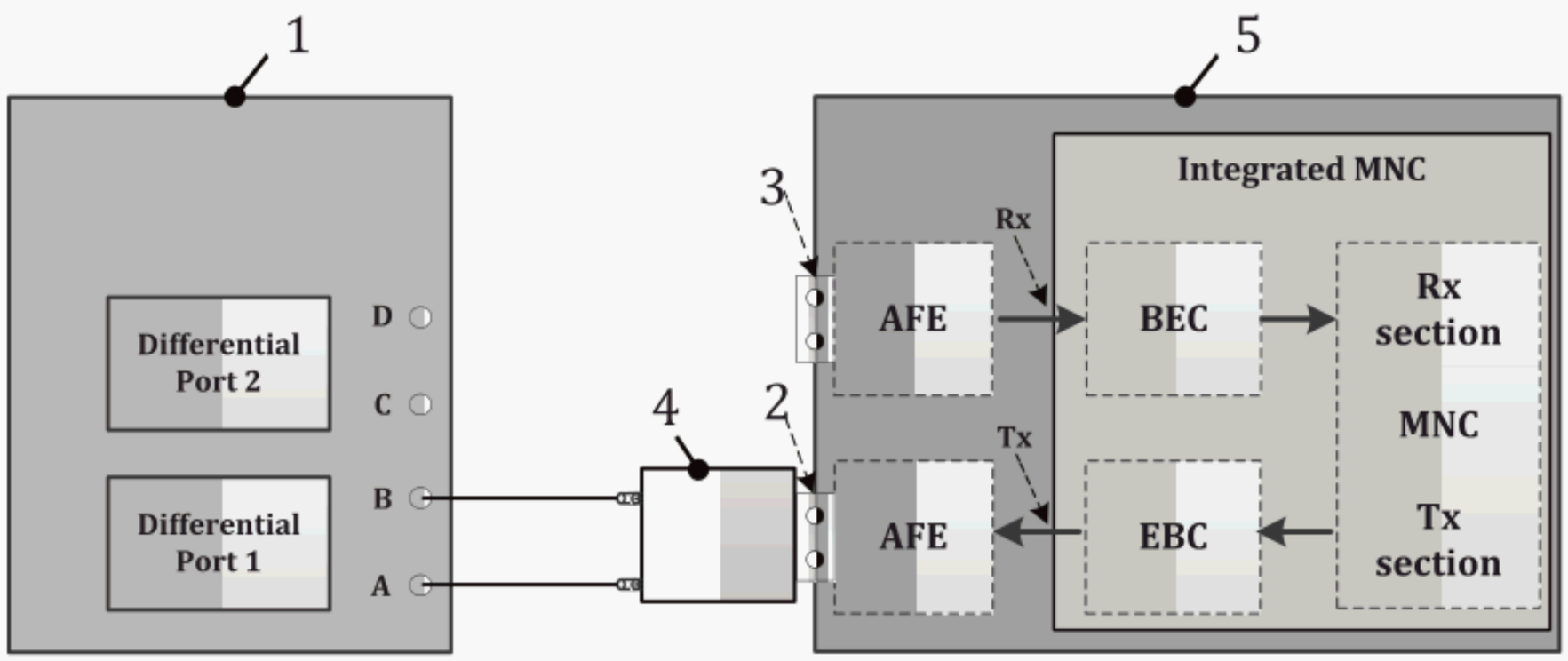
**Table 1 — Conditions for RL measurement of PCB interfaces**

| Test mode | Test case | Condition |
|---|---|---|
| SP2 silent mode | RL at SP2 | Test mode shall ensure:<br>— EBC impedance with AFE impairment detectable;<br>— EBC does not emit data transitions. |
| SP3 silent mode | RL at SP3 | Test mode shall ensure:<br>— BEC impedance with AFE impairment detectable;<br>— no valid data signal present, while stimuli from TDR or VNA may occur. |
| NOTE Based on the implementation of EBC and BEC functionality, the termination is detectable when the MNC is unpowered, powered, or powered and configured specifically. | | |

Figure 11 shows the measurement set-up for evaluation RL of PCB interfaces.




**Key**

1 VNA
2 SP2
3 SP3
4 test fixture
5 MOST device

**Figure 11 — Measurement set-up for evaluation RL of PCB interfaces**

ISO 21806-12 does not define specific requirements in resolution or scale of the frequency axis for RL.

NOTE It is solely in the responsibility of the supplier to apply appropriate settings.

Figure 12 shows a valid example plot of RL measurements for various PCB interfaces.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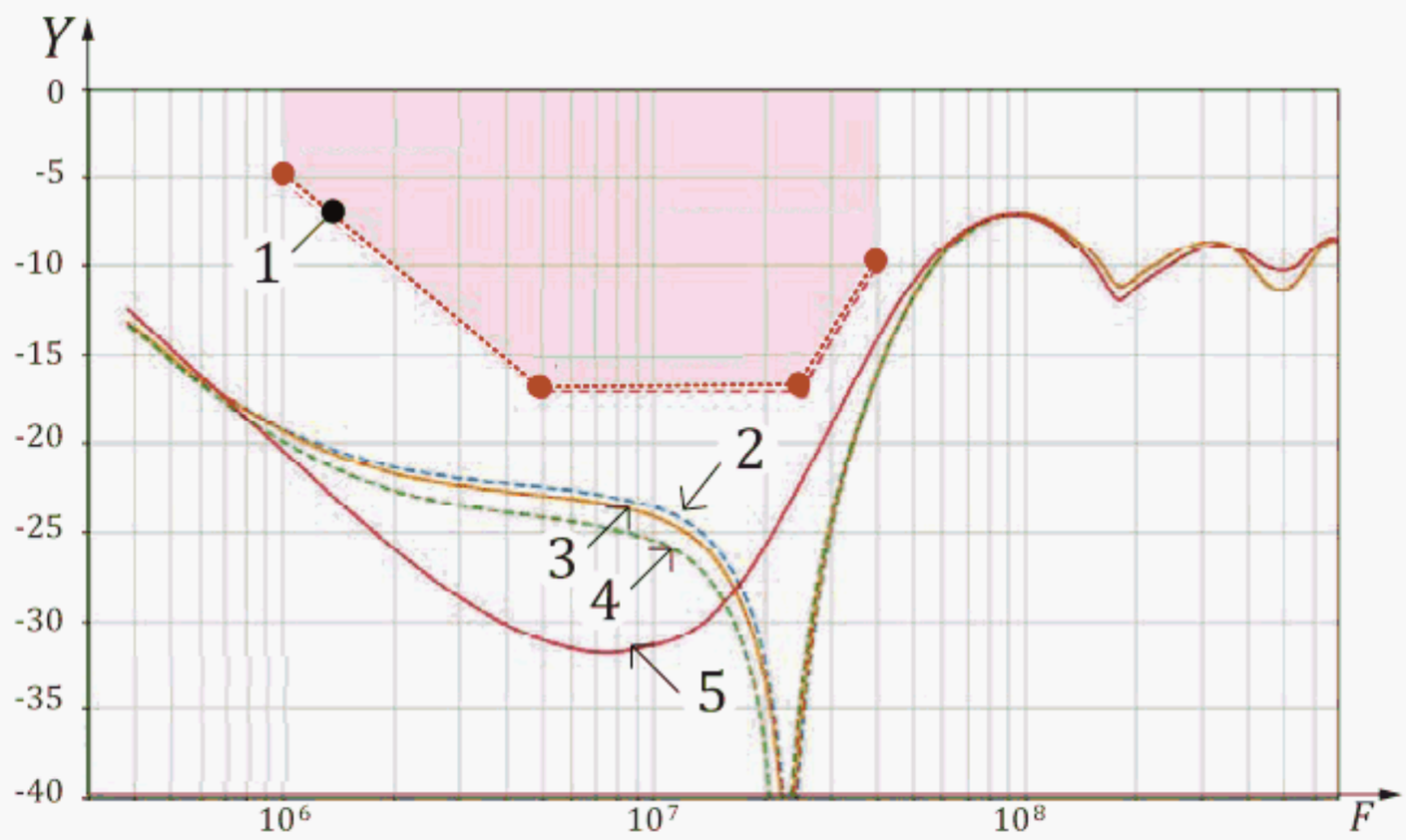


**Key**

| | |
|---|---|
| *F* | frequency [Hz] |
| *Y* | return loss [dB] |
| 1 | limit line |
| 2 | example 1 |
| 3 | example 2 |
| 4 | example 3 |
| 5 | example 4 |

**Figure 12 — Example RL measurement of PCB interfaces**

Time-domain reflectometry is another valuable method to evaluate impedance characteristic of such PCB interfaces. A TDR sends a pulse into the PCB interface and measures the response in magnitude and delay. The result usually is a plot of impedance over propagation time. For comparison with the specified limit line, the TDR result is converted to the frequency domain.

## 8.7 Receive tolerance

### 8.7.1 General

Evaluation of a receive tolerance means to apply worst case signals to SP3 and check the ability of the receiver to correctly recover clock and data. The challenge here is to find out what worst case means for a receiver, which conditions are relevant, and how to create such scenarios.

For better visibility, the block diagrams in 8.7.2, 8.7.3, and 8.7.4 specify simplified set-ups.

### 8.7.2 Pattern generator

The pattern generator is used to create MOST patterns, mainly for SP2. Such a pattern generator shall be able to create a signal that meets SP2 signal quality requirements (e.g. differential output signal, variation within extremes of timing distortion, adjustable output voltage).

Figure 13 shows the graphical element that represents a pattern generator.

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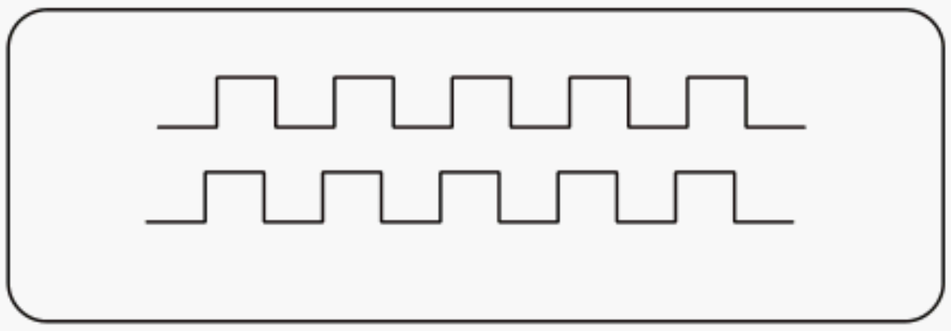

**Figure 13 — Pattern generator**

### 8.7.3 Arbitrary signal generator

The arbitrary signal generator is used to create MOST patterns, for SP2 and SP3.

The arbitrary signal generator is used to emulate pulse shape and timing, which includes signal variations as produced by a differential driver in combination with variations added by AFE or/and electrical interconnects.

Figure 14 shows the graphical element that represents an arbitrary signal generator.

**Figure 14 — Arbitrary signal generator**

### 8.7.4 Cable assembly or its analogue representation

The cable assembly or its analogue representation is used to emulate attenuation as produced by an electrical interconnect. This can be either real cables with known transfer characteristics, analogue modules emulating such cable transfer characteristic or combinations of both.

Figure 15 shows the graphical element that represents a cable assembly or its analogue representation.

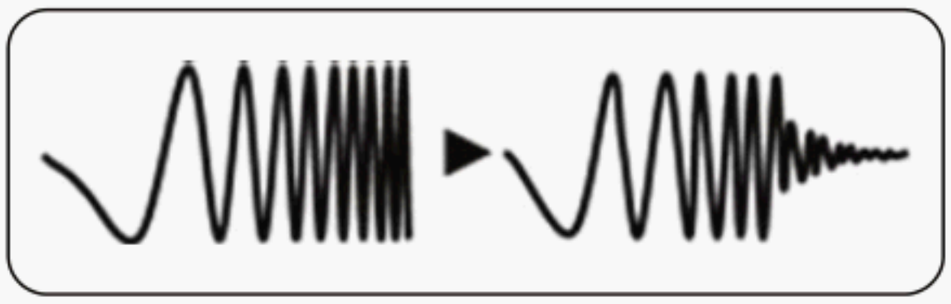

**Figure 15 — Cable assembly or its analogue representation**

### 8.7.5 Stimulus creation for SP3

Based on ISO 21806-12:2021, 9.4, the following impacts on signal quality at SP3 should be considered:

— valid MOST data starts from SP2 (all variations permitted, e.g. minimum and maximum voltage amplitude $V_{RMS}$, PSD, and jitter);

— signal is attenuated when travelling through the interconnect;

— some additional but minor losses occur at the interface between cable to PCB (SP3);


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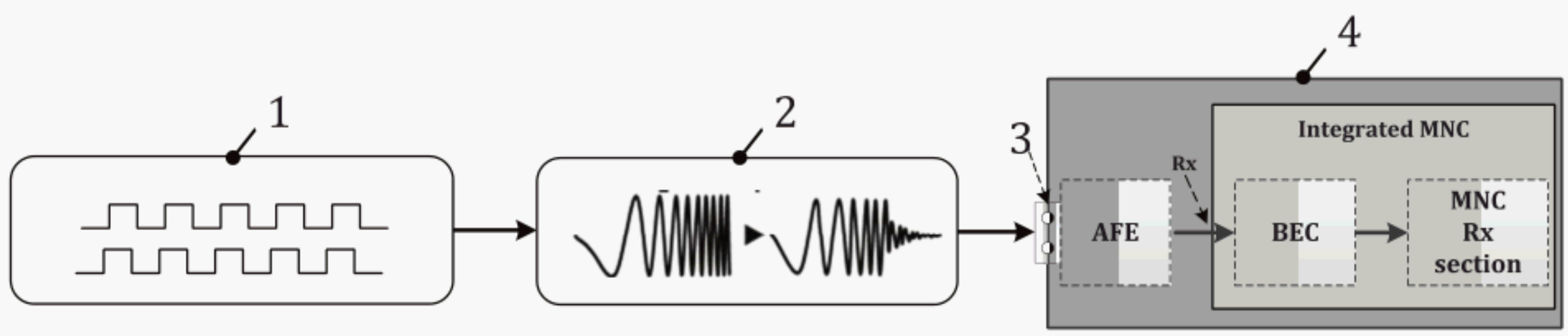
— for activity detection, other patterns (lower frequency content) than valid MOST patterns are used. Signal with lower amplitude or additional attenuation may be used for evaluating on-state/off-state thresholds.

There are three basic test set-ups which may be used to emulate above listed influences and stress an BEC under test. Table 2 specifies the configurations A and B.

**Table 2 — Basic test set-ups for configuration A and B**

| Cfg | EBC emulation (see key 1 of Figure 16) | Wire harness emulation (see key 2 of Figure 16) | BEC under test (see key 3 of Figure 16) |
|---|---|---|---|
| A | Pattern generator, signal conditioner, attenuator:<br>— square wave, with frequency < 10 kHz and up to 75 MHz;<br>— MOST50 bPHY stress pattern. | Frequency dependent attenuation:<br>— use real cables in various combinations, it requires pre-selected cables and components. | Apply stimulus to BEC;<br>check for sufficient/ requested tolerance at BEC. |
| B | Pattern generator, signal conditioner, attenuator:<br>— square wave, with frequency < 10 kHz, and up to 75 MHz;<br>— MOST50 bPHY stress pattern. | Frequency dependent attenuation:<br>— use specific circuitry, emulating cable characteristic with analogue filters;<br>— a few characteristics may be combined on one PCB. | Apply stimulus to BEC;<br>check for sufficient/<br>requested tolerance at BEC. |

Figure 16 defines the test set-up for BEC under test for configuration A and B.




**Key**

1 EBC emulation
2 wire harness emulation
3 SP3
4 MOST device: BEC under test

**Figure 16 — Test set-up for BEC under test – Configuration A and B**

Table 3 specifies the basic test set-up for configuration C.

**Table 3 — Basic test set-up for configuration C**

| Cfg | EBC and wire harness emulation (see key 1 of Figure 17) | BEC under test (see key 2 of Figure 17) |
|---|---|---|
| C | Using an arbitrary signal generator – combining signal generation with cable emulation:<br>— processing various patterns, including various signal conditions;<br>— adding frequency dependent attenuation;<br>— additional attenuation may be needed. | Apply stimulus to BEC;<br>check for sufficient/ requested tolerance at BEC. |

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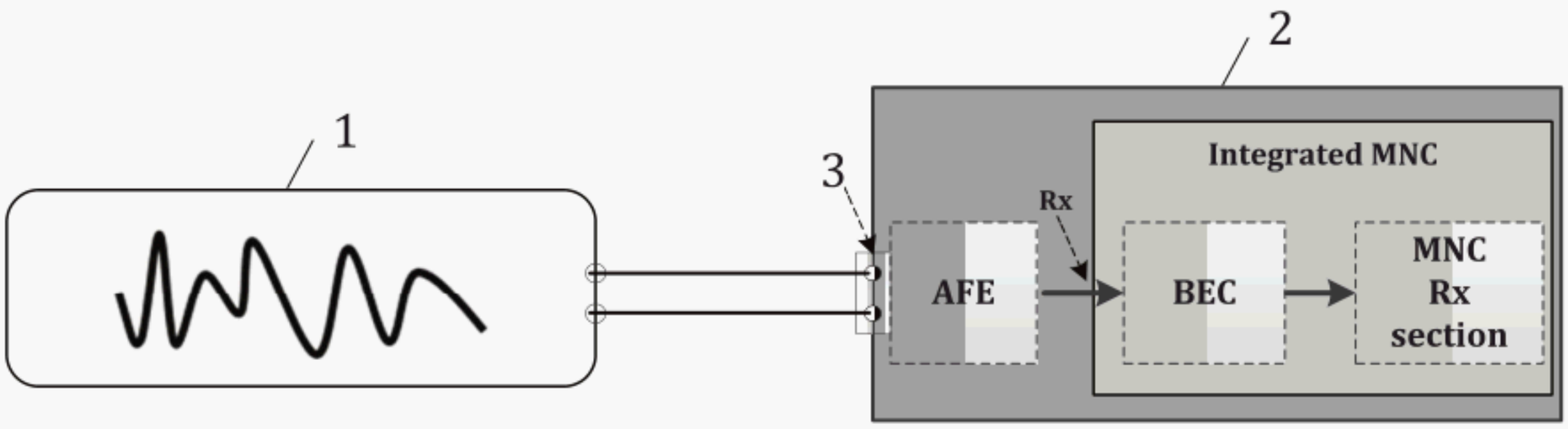


**Key**

1 EBC and wire harness emulation

2 MOST device: BEC under test

3 SP3

**Figure 17 — Test set-up for BEC under test – Configuration C**

If an attenuator is needed, use either:

— the differential signal from the generator and symmetrical attenuation on both signal lines (P and N), or

— the single ended signal from the generator, attenuator followed by BALUN (conversion into differential signal).

Table 4 describes the advantages and disadvantages of the suggested set-ups.

**Table 4 — Advantages and disadvantages of the suggested set-ups**

| Cfg | Advantage | Disadvantage |
|---|---|---|
| A, B | Wire harness/cable emulation can be re-used in real network-links, multi node networks, qualification testing, end-of-line testing, etc. | Fixed structure, not adaptable, practically low number of test scenarios are applicable. |
| C | Flexibility in generating multiple stress scenarios, easy adaptation for new configurations. | Not usable in real links, it cannot be reused in other test areas. |

# 9 Measurement of phase variation

## 9.1 General

Phase variation is caused by data stream noise and distortion in the time domain. Based on spectral content of the variation, sub-categories of phase variation are defined. Table 5 specifies the measurement of phase variation.

**Table 5 — Measurement of phase variation**

| Phase variation | Spectral limit |
|---|---|
| Wander | 0 Hz to 10 Hz |
| Transferred jitter (TJ) | Jitter between 10 Hz and the limit given by the jitter filter |
| Alignment jitter (AJ) | Jitter with spectral content above the limit given by the Golden PLL |

Figure 18 shows the sub-categories of phase variation.


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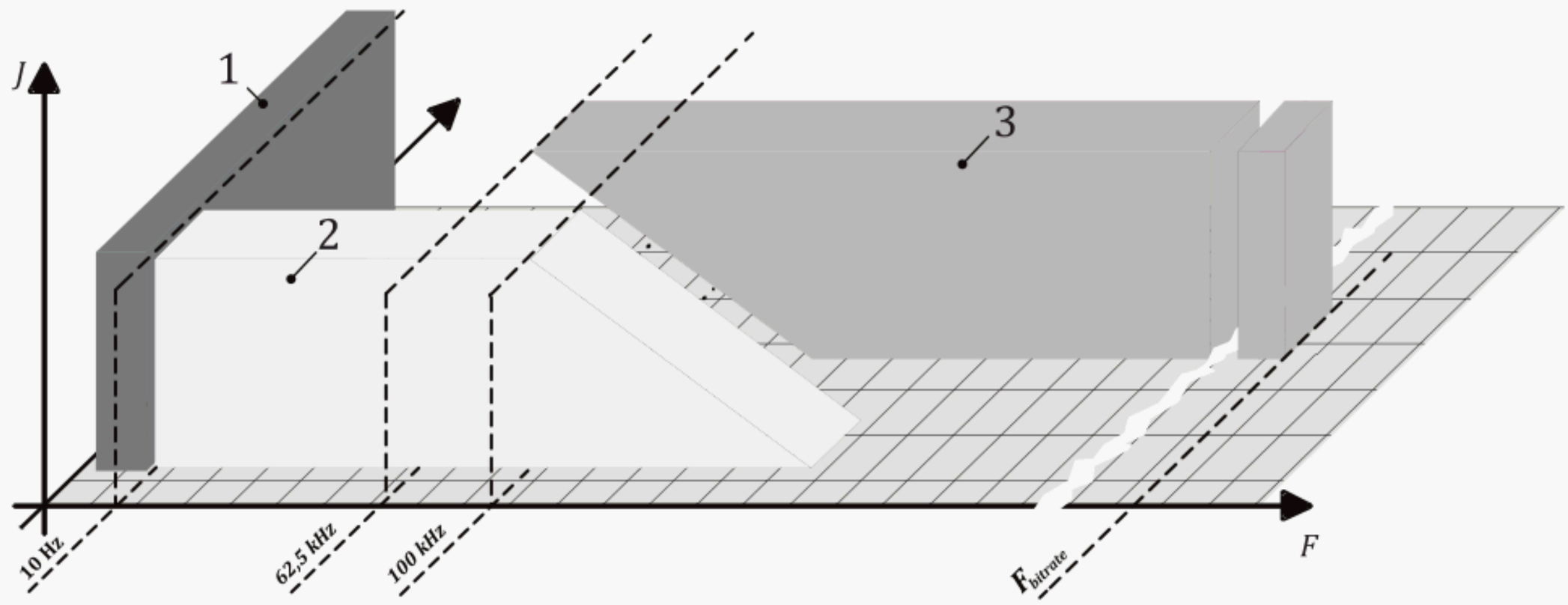


**Key**

*J* jitter

*F* frequency

1 wander

2 transferred jitter

3 alignment jitter

**Figure 18 — Sub-categories of phase variation**

MOST is a synchronous network; therefore, separating TJ and AJ is necessary. Due to the coding scheme used, a clock signal is embedded in the data stream. The receive unit of a node recovers the clock for sampling the received data stream from the data stream itself. The clock for sampling the output data of this node is derived from the recovered clock, which causes a certain correlation in phase between the receive unit and the output section of a node.

Clock recovery is realized by using a phase locked loop (PLL). The PLL enables the capability of tracking of phase variations. Phase variation in a lower spectral range on an incoming data stream is compensated by aligning the clock's phase accordingly. Therefore, low frequency jitter does not impact the data recovery. The clock for generating the output data, which is derived from the recovered input clock, is affected by the alignment process and may transfer phase variation from input to output.

High frequency jitter cannot be tracked by the PLL and leads to a temporary misalignment between sampling clock and input data, which limits the ability of error-free data recovery. A maximum misalignment (maximum alignment jitter) to be tolerated is defined with the eye masks for each specification point.

The dynamic characteristics of a PLL for a MOST node are covered by the physical layer specification with two definitions.

a) Golden PLL:

The Golden PLL is given in the form of a transfer function representing a low-pass filter. The Golden PLL serves two purposes.

1) It is used as a measurement tool for generating a time base, which is required for forming eye diagrams and determining AJ at each SP along a link. Based on the recovered UI clock an eye diagram is drawn. Eye masks, defined for each SP give the limits for AJ respectively.

It determines the behaviour of an MNC when jitter is applied to its input data. It marks the minimum capability of a PLL to track incoming phase variations. Jitter within the spectral range described by the low-pass filter is tracked by aligning the clock. Jitter beyond the spectral range described by the low-pass filter may lead to misalignment. The Golden PLL in

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combination with the eye mask for SP3 receiver tolerance specifies the minimum AJ tolerance of an MNC's receive section.

b) Jitter filter:

The jitter filter is given in the form of a transfer function representing a low-pass filter. It serves two purposes.

1) It is used as a measurement tool for extracting transferred jitter (TJ) out of the total jitter.

Additionally, it determines the worst-case jitter transfer characteristic over an MNC. Jitter below the spectral range described by the low-pass filter may be tracked by a PLL. The data stream being generated by this MNC and sampled with the recovered clock may transfer this low-frequency part of the total jitter.

## 9.2 Measuring alignment jitter

Table 6 specifies a procedure for detecting AJ in a data stream. Oscilloscopes, appropriate for the jitter measurements, are digital sampling oscilloscopes (DSO) with deep sampling memory and special software modules for serial data analysis.

**Table 6 — AJ measuring procedure**

| Action | Description |
|---|---|
| Acquiring a waveform | A probe (active differential or single-ended probe according to the SP under test) is connected to the IUT. The vertical scale is adjusted to achieve a sufficient vertical resolution. A sequence of the data stream ("waveform") is sampled into the oscilloscope's memory. |
| Clock recovery | The DCA-coded MOST50 data stream contains clock and data. In a first step, the oscilloscope shall extract the clock.<br>Data pulses range from 2 UI to 6 UI yielding five different pulse widths (2 UI, 3 UI, 4 UI, 5 UI, and 6 UI). The required clock has a cycle time of 1 UI, which is twice the bit rate (i.e. for a $\rho_{Fs}$ of 48 kHz, the bit rate is 49,152 Mbit/s and the UI clock is 98,304 MHz).<br>A method of extracting the UI clock from a waveform is a mandatory function to be provided with the oscilloscope. In a first step, the recovered UI clock is a linear approximation that fits best to the acquired waveform in terms of phase and frequency. MOST50 specifies that the Golden PLL is applied on positive edges of the data stream only; the approximation of the clock's phase shall be performed with regard to the rising edges of the data stream only. |
| Applying low-pass filter given by Golden PLL | Once a first derivate of the UI clock is approximated, there might still be phase differences between rising data edges and the recovered UI clock, called time interval errors. Applying the low-pass filter (given by the Golden PLL) to the sequence of consecutive time interval errors results in a filtered phase deviation sequence. This sequence represents the minimum capability of the MNC to track incoming phase variations by adjusting the phase of its sampling clock. In order to recover this sampling clock, phases of the first derivate of the UI clock shall be compensated by the sequence of filtered phase deviations.<br>The resulting new UI clock, which is used for further calculations, now represents the base UI clock incorporated in the data stream, overlaid with a modulation in phase that follows phase variations in the data stream. However, modulation capability is limited in spectrum given by the Golden PLL. |
| Calculating alignment jitter | Alignment jitter is the phase deviation between any edge of the waveform and the correlating transition of the recovered UI clock. Calculating the misalignment between clock and data for each data transition and drawing the successive phase deviations over runtime in a graph result in an "AJ track", which is the base for further evaluations. Calculating a frequency distribution out of the phase deviation results in an "AJ jitter histogram". |


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**Table 6** *(continued)*

| Action | Description |
|---|---|
| Drawing the eye diagram | For drawing the eye diagram, the waveform is sliced into intervals of 1 UI length aligned with the UI clock. The sliced waveform segments plus some overhead (i.e. 0,25 UI on both sides) are overlaid in one graph.<br>As shown in Figure 19, each transition is drawn twice, first on the left side and second on the right side of the diagram. Therefore, the statistical distribution of transitions at the threshold level is identical on both sides of the eye diagram.<br>Duty cycle distortion (DCD), if it exists, shifts the eye towards the mask. In the shown example, logic 0 pulses are shorter than logic 1 pulses. The UI clock is referenced to rising edges, which causes the rising edges to be adjusted to the UI borders, while the falling edges are shifted by the amount of the DCD. |
| Pass/fail test using eye masks | Signal integrity shall be checked using eye masks. The masks are defined as keep-out areas; each violation is interpreted as a bit error.<br>The masks are defined by hexagons with points A, B, C, D, E, and F. Points A and D are limiting AJ while B, C, E, and F build constraints for amplitude and pulse shape. |
| Bit error rate | The requested BER of $10^{-9}$ is represented by an eye diagram showing at least $10^9$ bits without violation of the mask.<br>1 bit is represented in 2 UI. Therefore, at least $2 \times 10^9$ samples are required.<br>Alternatively, statistical methods for accelerated testing of BER are acceptable. Selection of a method for extrapolation and definition of the required database to be measured for extrapolation is in the responsibility of the user. |

Figure 19 shows the example 1 of measuring alignment jitter. The UI clock is fitted in frequency and phase to the waveform. Remaining phase deviations are marked in the diagram. Phase deviations for rising edges are shown in the time interval error graph.

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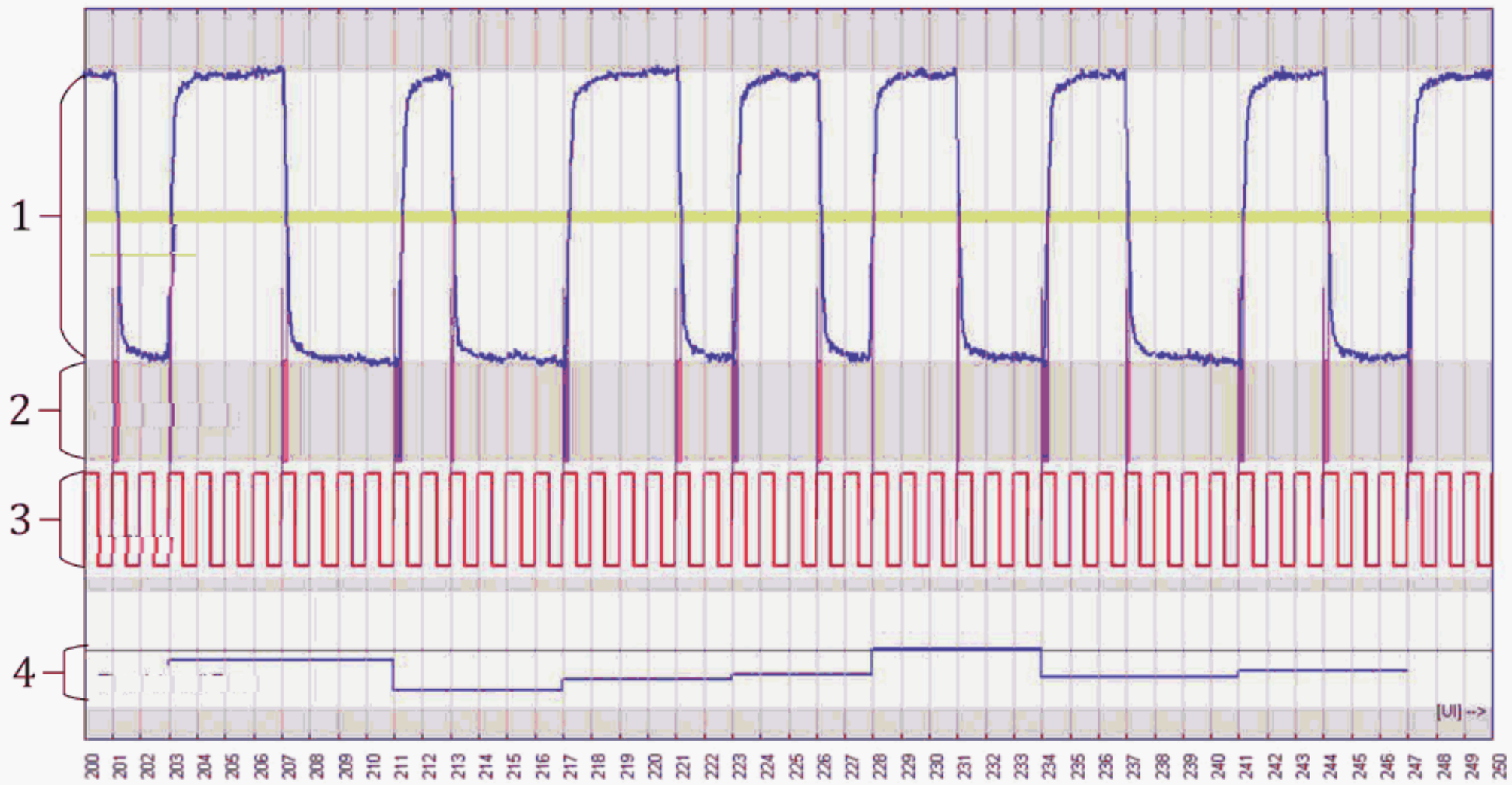


**Key**

1 waveform input signal

2 phase deviation

3 UI clock

4 time interval error

**Figure 19 — Example 1 of measuring alignment jitter**

NOTE In many oscilloscopes, visualization of the recovered UI clock is not possible.

Figure 20 shows the example 2 of measuring alignment jitter. The sliced waveform segments are marked in the waveform graph. The segments are overlaid in eye diagrams.


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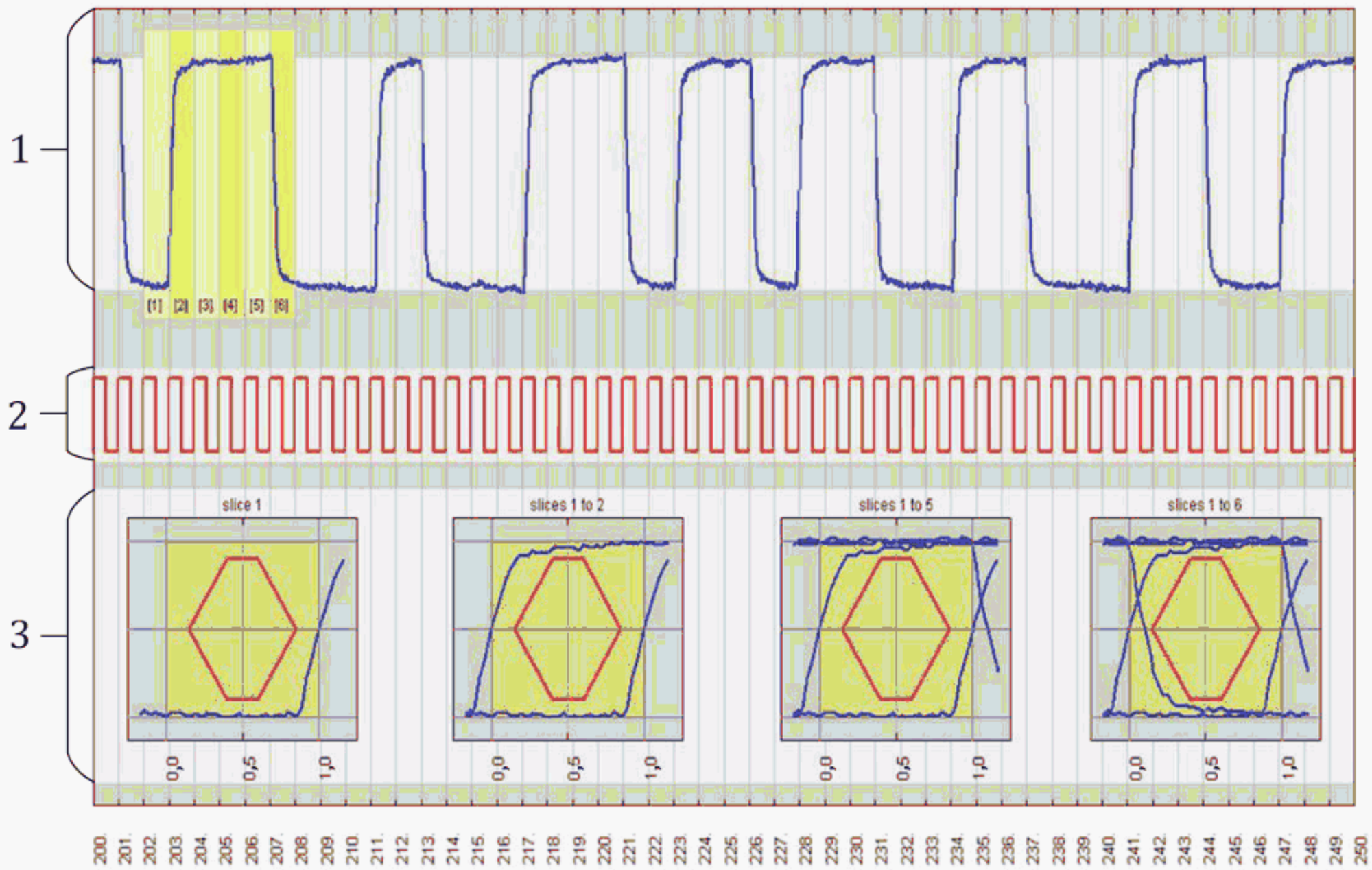


**Key**

1 waveform input signal

2 UI clock

3 eye diagrams

**Figure 20 — Example 2 of measuring alignment jitter**

## 9.3 Measuring transferred jitter

Table 7 specifies a procedure of determining TJ in a measured data stream.

**Table 7 — Measuring transferred jitter**

| Action | Description |
|---|---|
| Acquiring a waveform | For this measurement, the maximum available sampling memory of the oscilloscope shall be used. A probe (active differential or single-ended probe according to the SP under test) is connected to the IUT interface. The vertical scale is adjusted to achieve a sufficient vertical resolution; see 8.1 and 8.2. A sequence of the data stream, which is referred to as waveform, is sampled into the oscilloscope's memory.<br>TJ is defined in the spectrum from 10 Hz (beyond wander) to 100 kHz. The determination of this jitter is limited by the size of memory of the oscilloscope. |

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**Table 7** *(continued)*

| Action | Description |
|---|---|
| Clock recovery | Similar to the AJ measurement procedure, the clock shall be extracted. Clock separation is provided by an oscilloscope internal function.<br>Similar to the AJ measurement procedure, the recovered UI clock is a linear approximation that fits best to the acquired waveform in terms of phase and frequency. The approximation of the clock's phase shall be performed with regard to the rising edges of the data stream only.<br>In contrast to the AJ measurement procedure, a PLL functionality for tracking phase variations is basically not necessary. Small deviations in the detected bit-rate might grow to a significant phase mismatch over the length of the acquired waveform and, therefore, affect further results. To enable a robust measurement procedure, it is tolerable to apply a PLL with lowest possible bandwidth (as close as possible to 10 Hz). |
| Extracting transferred jitter | Jitter is the phase deviation between an edge of the waveform and the correlating transition of the recovered UI clock. For transferred jitter, only phase variations coming with rising edges of the waveform are relevant because only these deviations are tracked by the PLL and impact the recovered clock's phase.<br>Calculating the misalignment between clock and data for rising edges and drawing the successive phase deviations over runtime in a graph result in a "jitter track".<br>Successive phase deviations appear in pulse time intervals (2 UI, 3 UI, 4 UI, 5 UI, and 6 UI), which correspond to the theoretical maximum jitter frequencies up to 150 MHz. With respect to the focused spectral range 10 Hz to 200 kHz, it is acceptable to reduce the amount of jitter values by skipping samples in regular intervals. The reduction might be helpful for accelerating the measurement process.<br>In the next step, this jitter track (optionally reduced) shall be low passed, using the transfer function given with the jitter filter definition, which results in the "filtered jitter". |
| Calculating transferred jitter | Transferred jitter is calculated by accumulating the phase deviations of the filtered jitter by using the root-mean-square method ($v_{\mathrm{RMS}}$) as specified in Formula (4).<br>If the spectrum of the filtered jitter contains values below 10 Hz (e.g. caused by a constant phase mismatch between clock and data), the standard deviation as specified in Formula (5) may be calculated instead of the $v_{\mathrm{RMS}}$. |

$$v_{\mathrm{RMS}} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} v_i^2} \tag{4}$$

where

$v_{\mathrm{RMS}}$ is the transferred jitter, calculated using the root-mean-square method;

$N$ is the number of samples;

$i$ is the index of summation;

$v$ is the phase deviation.

$$S_{\mathrm{Dev}} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} (v_i - v_{\mathrm{mean}})^2} \tag{5}$$

where


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$S_{Dev}$ is the standard deviation;

$N$ is the number of samples;

$i$ is the index of summation;

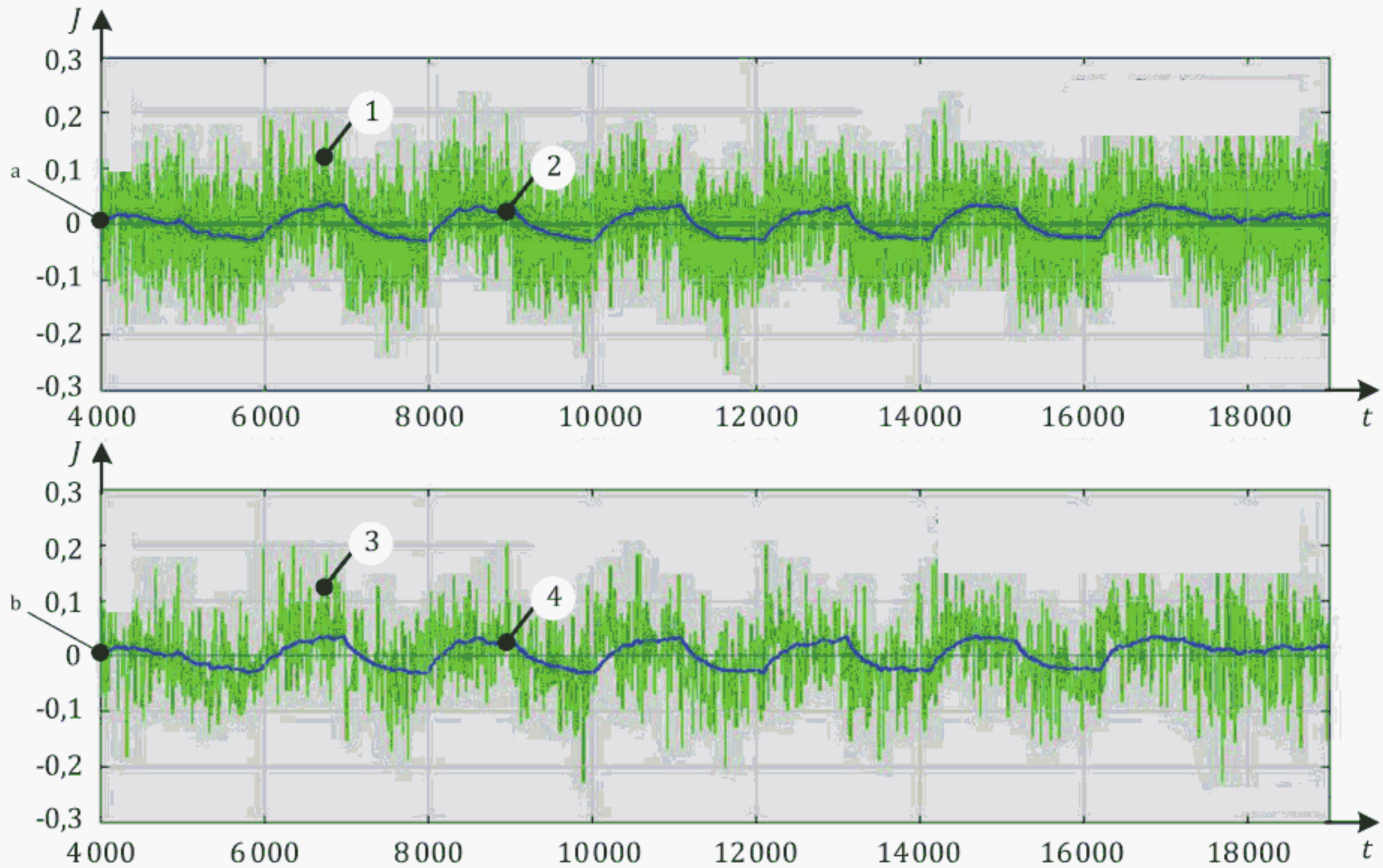
$v$ is the phase deviation;

$v_{mean}$ is the mean (average) phase deviation.

EXAMPLE of measuring transferred jitter

— Figure 21 upper graph: successive phase deviations are shown over runtime (jitter unfiltered), weighting with the jitter filter leads to the low-passed version (jitter filtered);

— Figure 21 lower graph: successive phase deviations but reduced by factor 10 are shown over runtime (jitter unfiltered), weighting with the jitter filter leads to the low-passed version (jitter filtered).




**Key**

$t$ time [UI]

$J$ jitter [UI]

1 jitter unfiltered (green signal)

2 jitter filtered (blue signal)

3 jitter unfiltered, reduced by 1/10 (green signal)

4 jitter filtered, reduced by 1/10 (blue signal)

a Successive phase deviations are shown over runtime (jitter unfiltered), weighting with the jitter filter leads to the low-passed version (jitter filtered).

b Successive phase deviations but reduced by factor 10 are shown over runtime (jitter unfiltered), weighting with the jitter filter leads to the low-passed version (jitter filtered).

**Figure 21 — Example of measuring transferred jitter**

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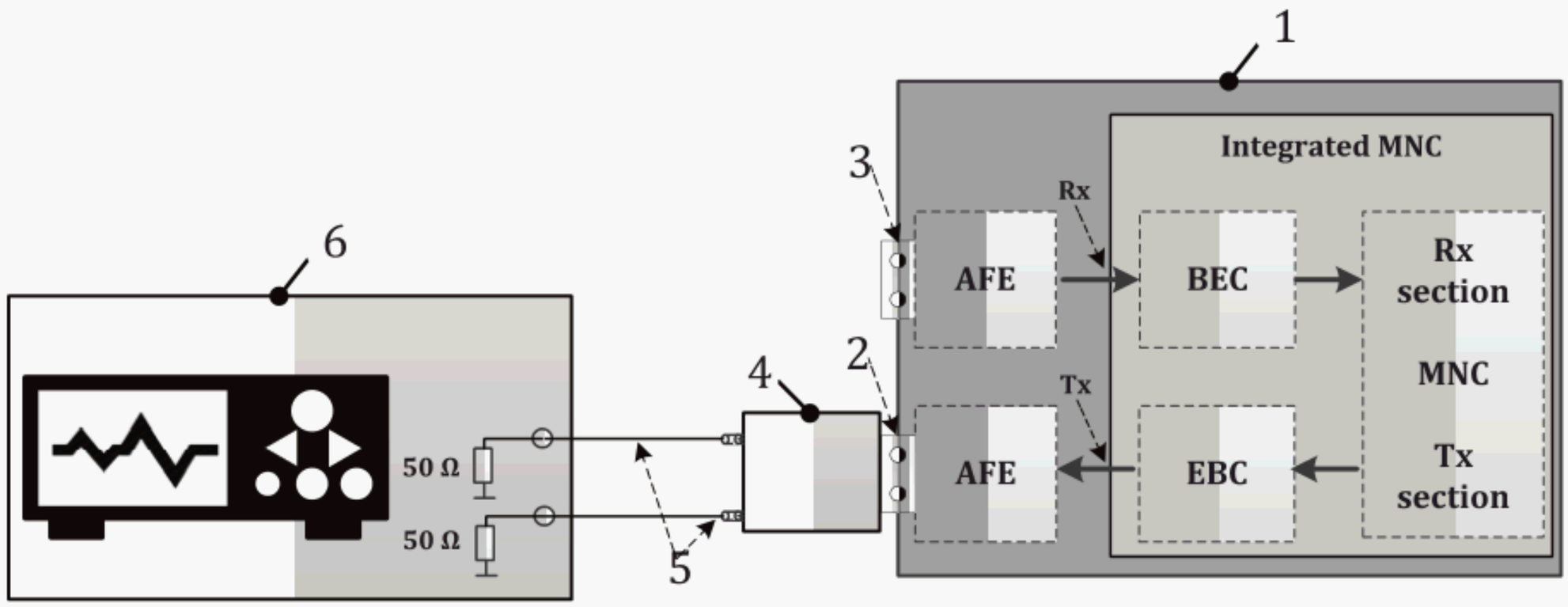


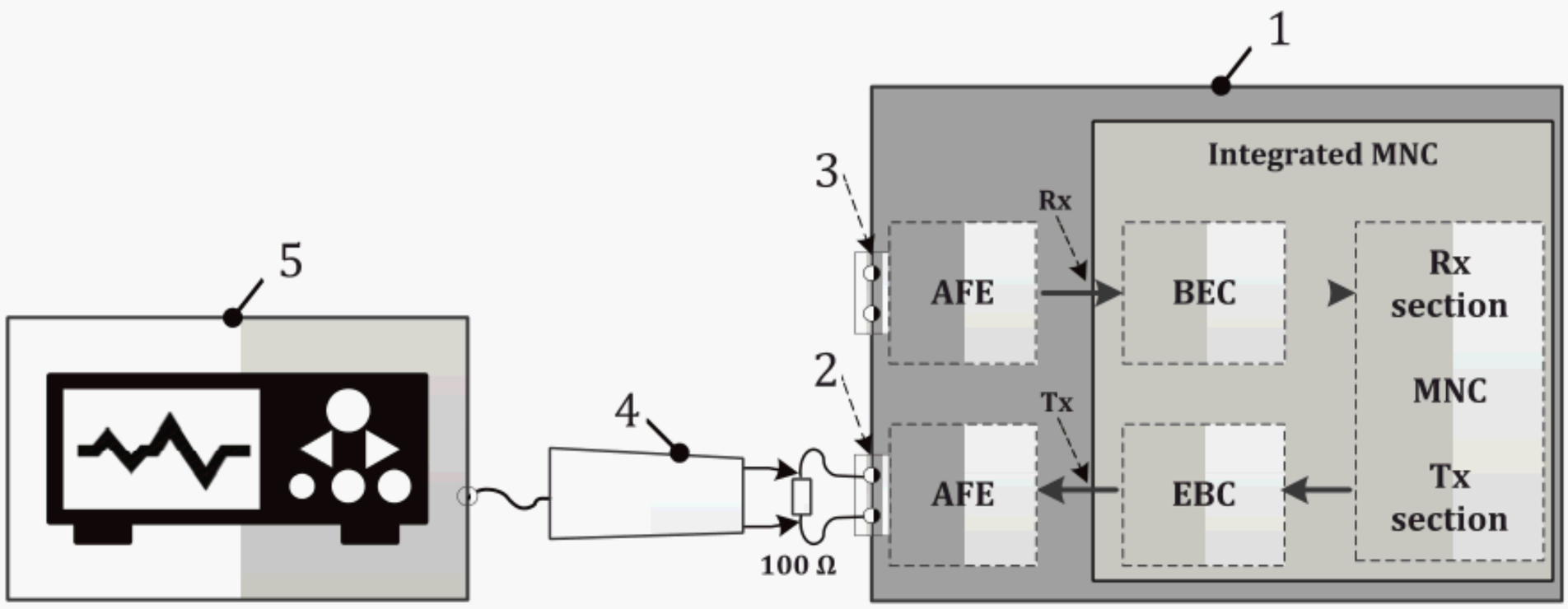

**Key**

1 MOST device
2 SP2
3 SP3
4 test fixture
5 single ended cable
6 oscilloscope

**Figure 22 — Measurement set-up for SP2 – Option 1**

Option 2: add a 100 Ω termination to the differential signal at SP2 and use a differential probe, connected to an oscilloscope channel.

Figure 23 shows the measurement set-up for SP2, option 2.




**Key**

1 MOST device
2 SP2
3 SP3
4 differential probe
5 oscilloscope

**Figure 23 — Measurement set-up for SP2 – Option 2**

Figure 24 shows an example of the SP2 eye diagram, option 2.

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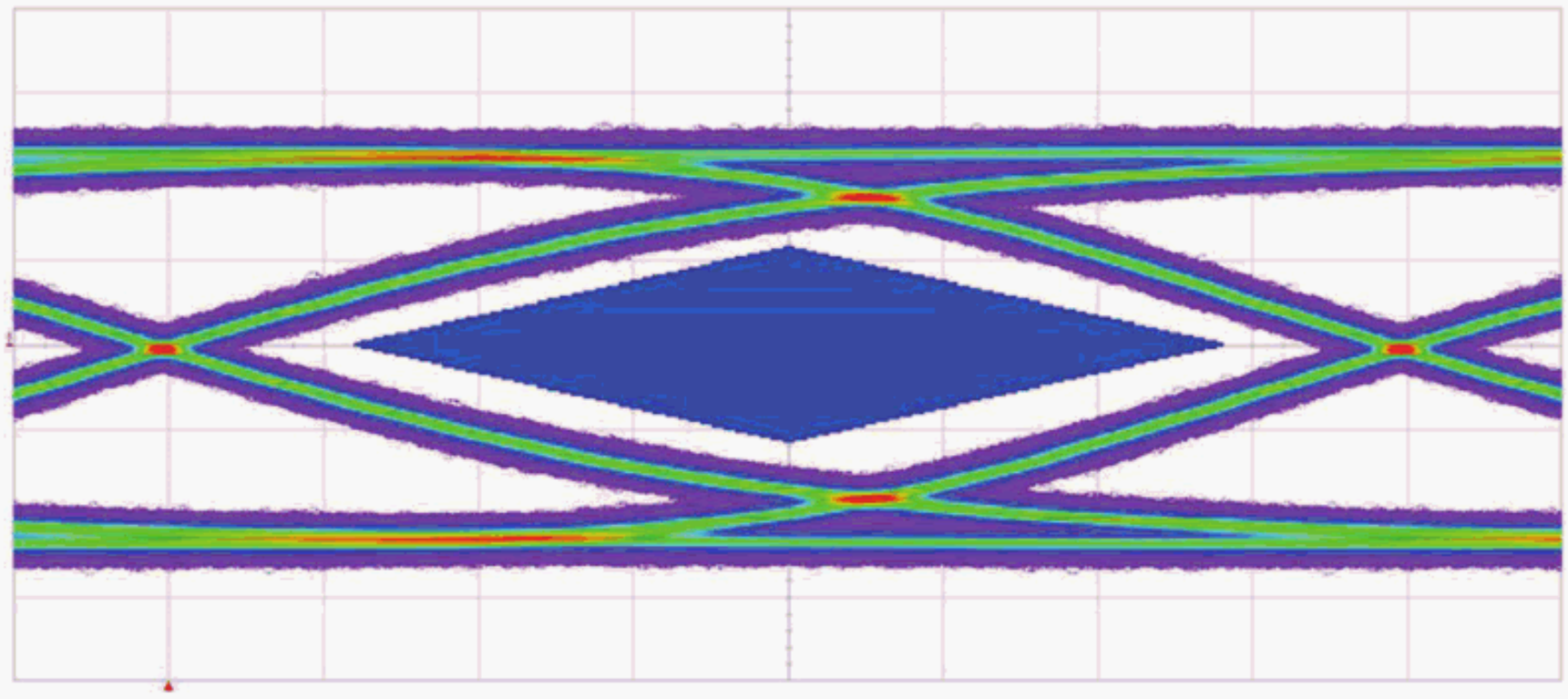

**Figure 24 — Example of the SP2 eye diagram – Option 2**

Compensation of DC offset is performed as follows.

DC offset in the measurements shall be minimized as it might indirectly compromise timing-parameter and RMS signal voltage amplitude results. With shown set-up options, put the EBC into test mode "SP2 silent mode". The differential signal swing is zero and the common mode, due to AC-coupling in the signal path is expected to be zero. Any deviation of the common mode from zero is DC offset and shall be compensated.

## 10.3 Set-ups for SP3 link quality

MNC and AFE provide an SP2 signal. Alternatively, a signal generator can be used. Table 9 specifies the set-ups for SP3 link quality.

**Table 9 — Set-ups for SP3 link quality**

| Test mode | Test case | Condition |
|---|---|---|
| MOST50 bPHY stress pattern | SP2 link quality:<br>— signal voltage amplitude $V_{RMS3}$;<br>— alignment jitter, according to eye mask $A_3$ to $D_3$;<br>— transferred jitter $J_{tr3}$. | Data signal at SP2 provides data content as specified for MOST50 bPHY stress pattern. |
| SP2 silent mode | DC offset compensation for SP3 link quality | Test mode shall ensure:<br>— signal generator or EBC impedance with AFE impairment detectable;<br>— signal generator or EBC does not emit data transitions. |

Two options to connect to the oscilloscope are shown.

Connect SP3 directly to two 50 Ω terminated oscilloscope channels and use the oscilloscope's MATH functions to create the differential signal. A test fixture is being used to connect the differential cable system to the single ended measurement equipment. For details see Annex C.

Figure 25 shows the test set-up for SP3 link quality, option 1.


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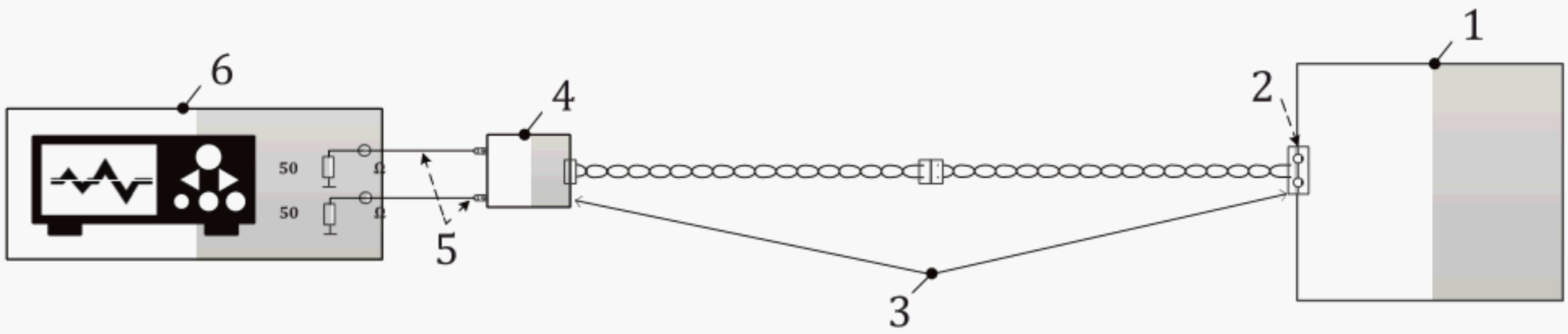



**Key**

1 ECU, SP2 (real MNC and AFE) producing required pattern or signal generator producing required pattern and signal characteristic

2 SP2

3 interconnect under test

4 test fixture

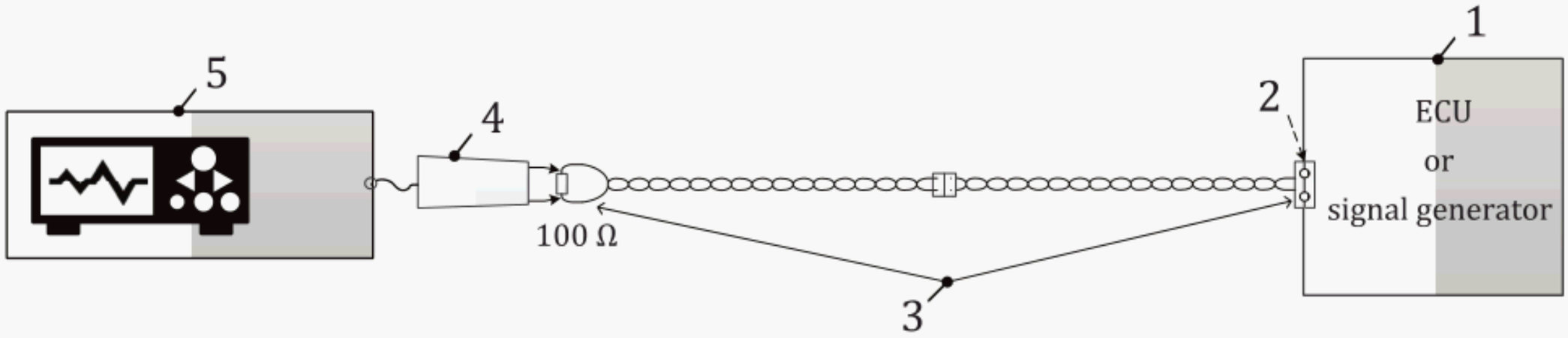
5 single ended cable

6 oscilloscope

**Figure 25 — Test set-up for SP3 link quality – Option 1**

Alternatively, add a 100 Ω termination to the differential signal at SP3 and use a differential probe, connected to an oscilloscope channel.

Figure 26 shows the test set-up for SP3 link quality, option 2.




**Key**

1 ECU, SP2 (real MNC and AFE) producing required pattern or signal generator producing required pattern and signal characteristic

2 SP2

3 interconnect under test

4 differential probe

5 oscilloscope

**Figure 26 — Test set-up for SP3 link quality – Option 2**

Figure 27 shows an example of the SP2 eye diagram, option 2.

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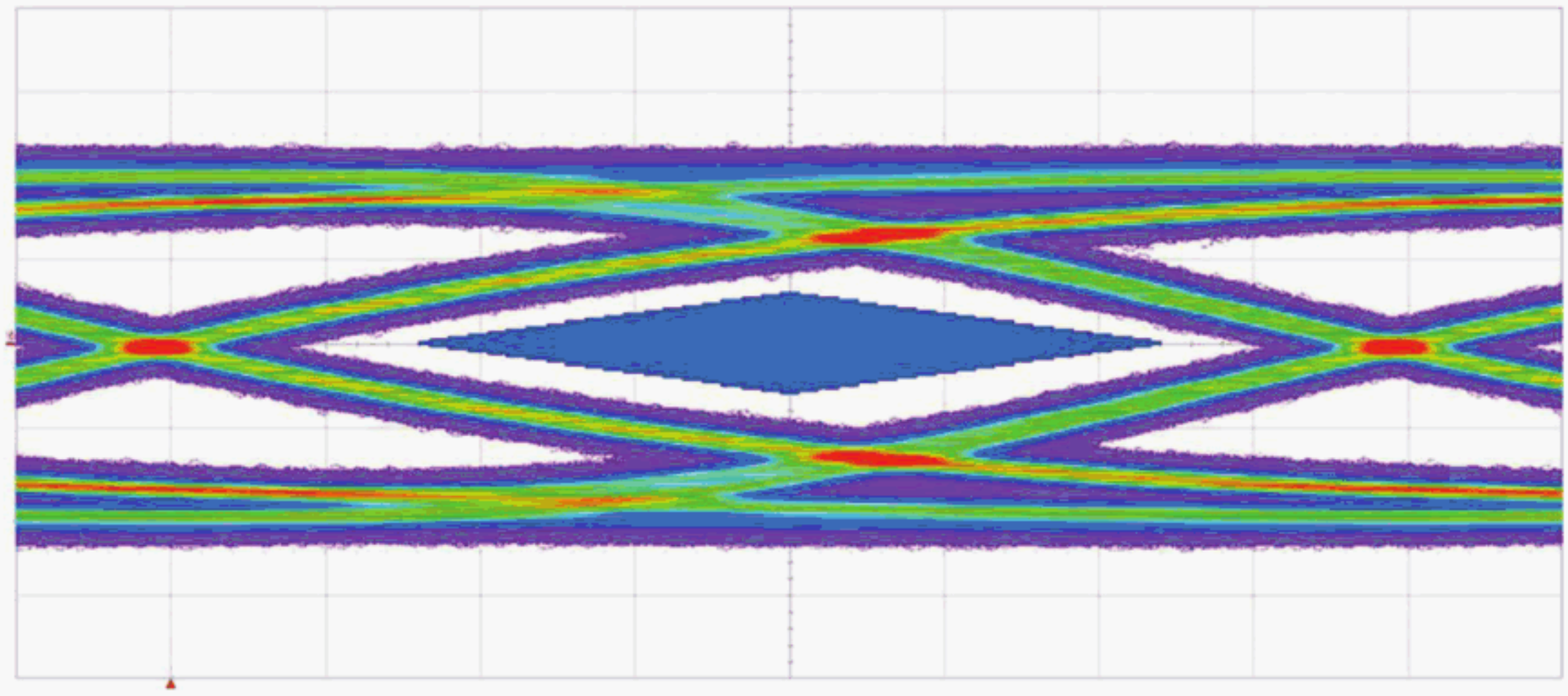


**Figure 27 — Example of the SP2 eye diagram – Option 2**

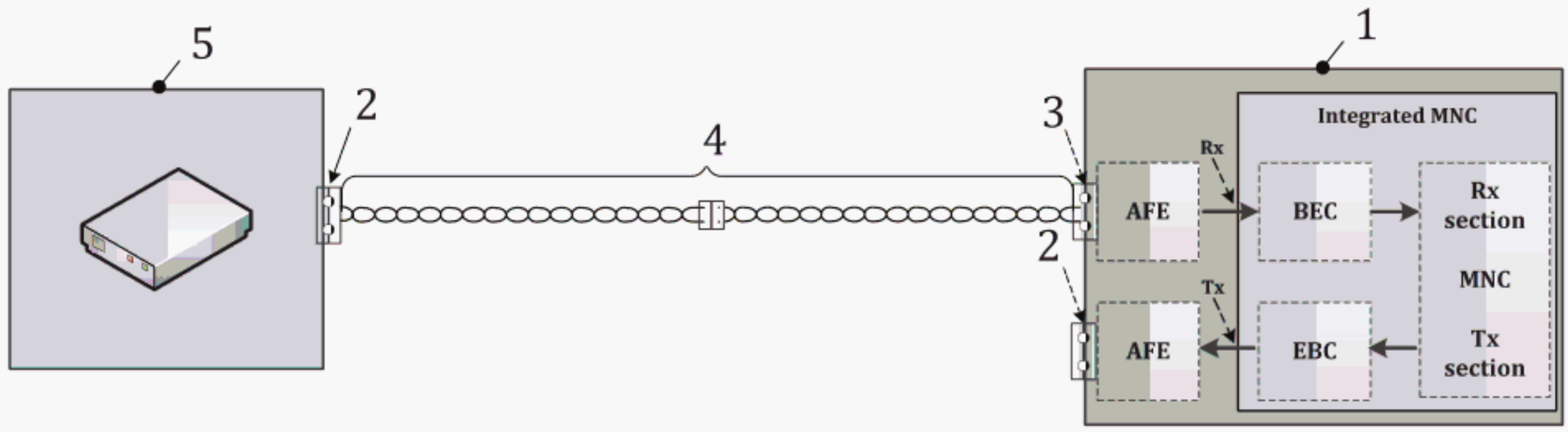
Compensation of DC offset is performed as follows.

DC offset in the measurements is minimized as it may indirectly compromise timing-parameter and signal voltage amplitude $V_{RMS}$ results. With shown set-up options, the EBC or signal generator is set to test mode "SP2 silent mode". The differential signal swing at SP2 is zero and the common mode, due to AC-coupling in the signal path, is supposed to be zero. Any deviation of the common mode from zero is DC offset and needs to be compensated.

## 10.4 Set-ups for SP3 receive tolerance

This subclause discusses SP3 receive tolerance set-ups. These set-ups are targeting the ability of an ECU receive (Rx) section to recover clock and data from a stressed input signal. General options to generate stressed signals is discussed in 8.7.5.

Figure 28 shows the test set-up for SP3 receive tolerance, options A and B.




**Key**

1 MOST device

2 SP2

3 SP3

4 worst case cable assemblies

5 ECU, SP2 (real MNC and AFE) producing required pattern or signal generator producing required pattern and signal characteristic

**Figure 28 — Test set-up for SP3 receive tolerance – Option A and B**


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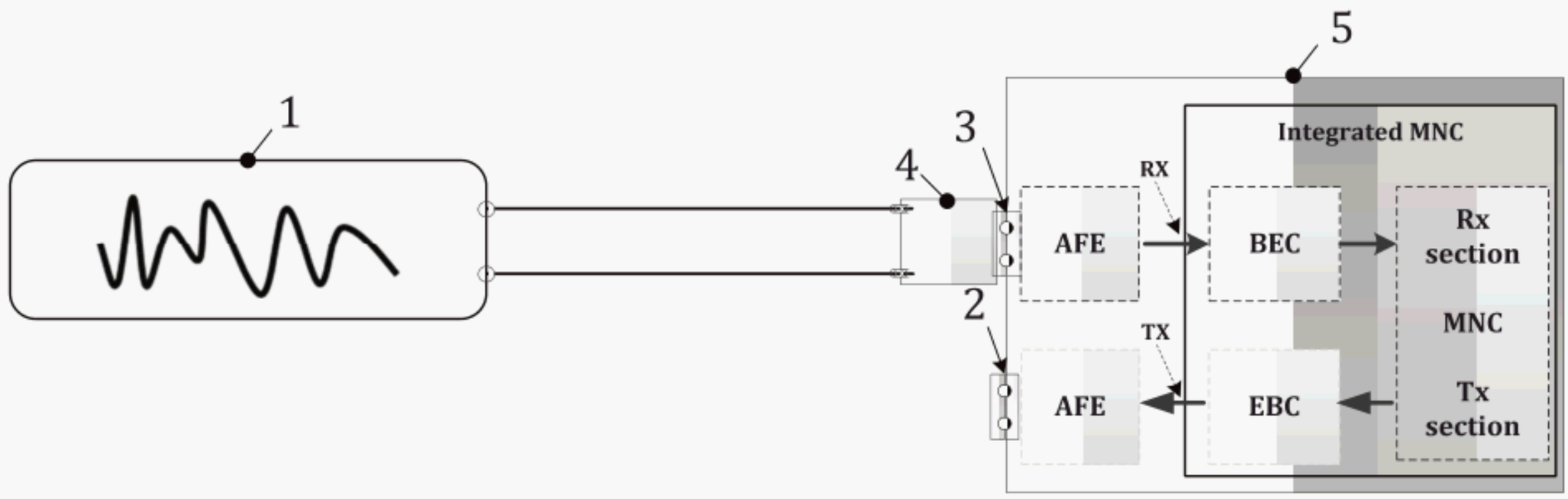
Figure 29 shows the test set-up for SP3 receive tolerance, option C.




**Key**

1 arbitrary signal generator
2 SP2
3 SP3
4 test fixture
5 MOST device

**Figure 29 — Test set-up for SP3 receive tolerance – Option C**

# 11 Power-on and power-off

## 11.1 General

This subclause defines several possible test set-ups and sequences to exercise as many functional EBC and BEC requirements as possible and also provides guidelines for the interpretation of results.

All test sequences shall be performed for the minimum, typical, and maximum of the operating voltage according to operating conditions specified in 6.1.

All test sequences shall be performed for the minimum, typical, and maximum temperature specifications.

When testing MOST modules (EBC and BEC in one enclosure), crosstalk effects should be considered. When testing one MOST module, the other MOST modules shall be active.

Some of the parameters specified in ISO 21806-12:2021, Clause 10 can be measured ($t_{STATF}$, $t_{STATR}$, etc.); other parameters ($t_{ON2}$, $t_{OFF2}$, $t_{ON4}$, etc.) determine relations between operation states and do not have distinct boundaries. For the parameters that cannot be measured, this clause specifies test sequences including a timeout, which represents the maximum and minimum time interval allowed for the respective parameter. The end of the interval is marked as action point in the signal charts (e.g. Figure 31). It defines the time for a state validity evaluation.

For example, $t_{ON2}$(max.) time after the /RST signal transitions to logic 1, start evaluating the SP2 signal quality to check for conformance to the requirements for valid MOST data.

Measuring electrical parameters such as LVTTL conformance is beyond the scope of this document and not discussed in detail herein, but some guidelines are given to facilitate proper parameter interpretation.

Testing of activity detection for EBC is described in 11.2, followed by descriptions for BEC in 11.3.

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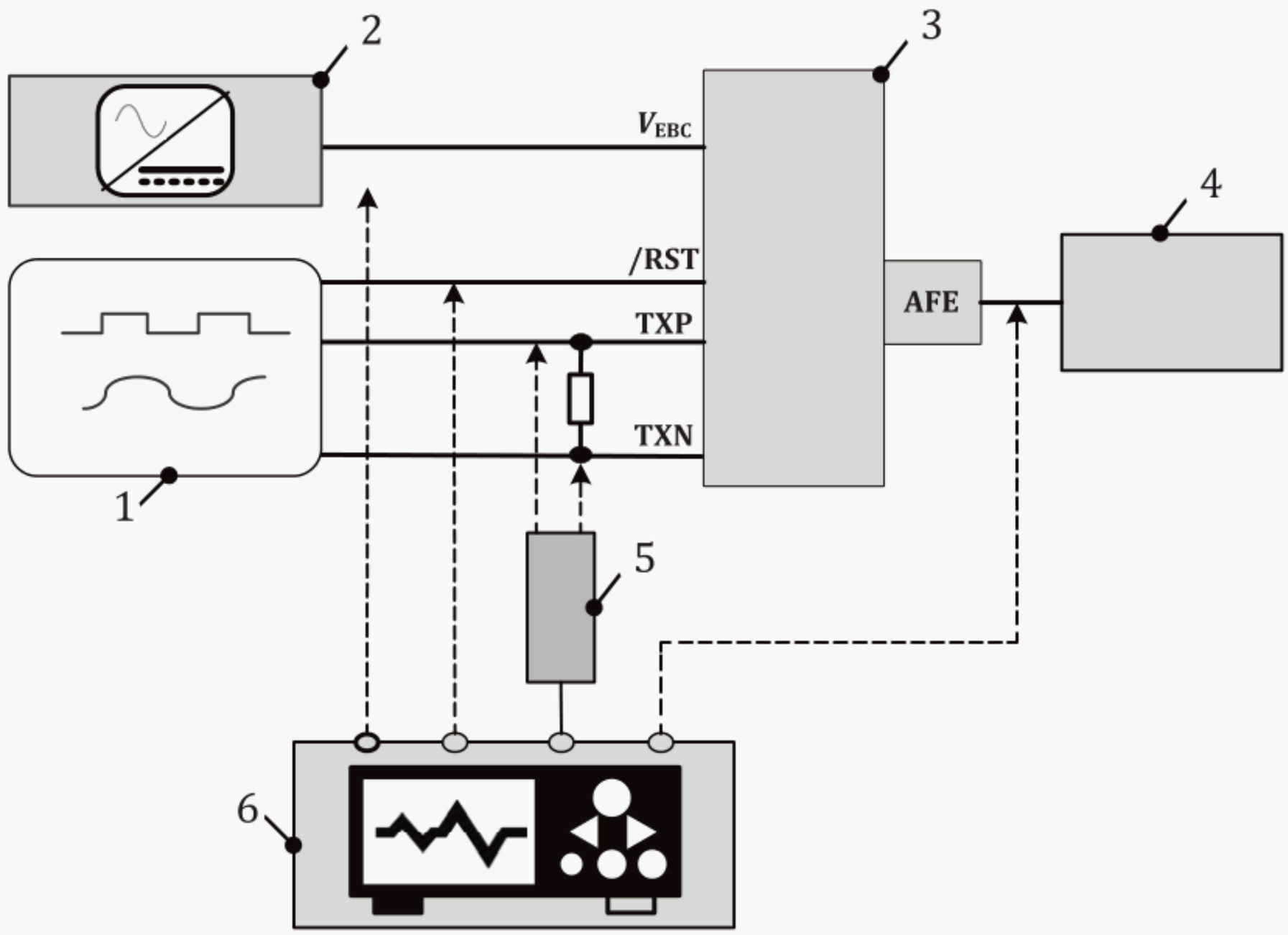
Testing of BEC's activity detection includes the full variety of scenarios being influenced by outer conditions, such as BEC power state requirements, SP2 signal performance of the preceding node, or attenuation of the electrical interconnect.

## 11.2 Measuring EBC parameters

### 11.2.1 Measuring EBC parameters – Test set-up

Figure 30 shows an example of the test set-up for measurement of the EBC's power-on and power-off parameters.




**Key**

1 signal generator
2 programmable power supply
3 IUT (BEC)
4 termination
5 differential probe
6 oscilloscope

**Figure 30 — Set-up for measuring EBC power-on and power-off parameters**

The main parts of the set-up are:

— the IUT is fitted according to the manufacturer's recommended set-up;

— the stimuli are directly fed into the MNC, while the output signal is measured at SP2; to exclude AFE impact, the output signal can also be measured directly at the MNC's TX pins;

— the signal generator (i.e. pattern generator or arbitrary signal generator) is used to produce the stimuli, produce a trigger signal, and control the EBC power supply;

— differential 100 Ω termination is used;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— the oscilloscope captures input and output signal data;

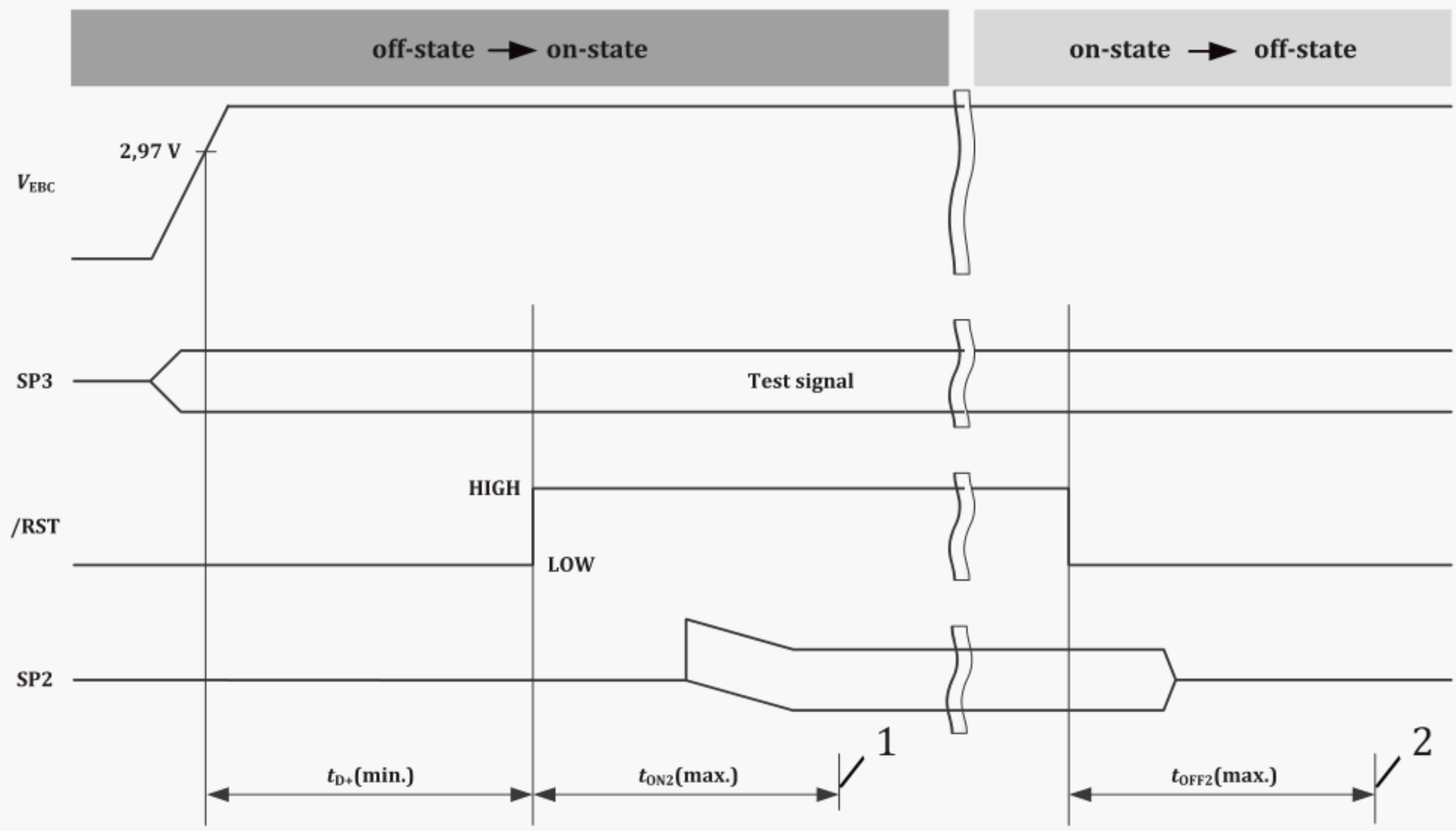
— the programmable power supply turns the EBC power on and off, and provides the desired supply voltage.

### 11.2.2 Measuring EBC parameters – Signal charts

The signal charts represent the graphical view of test sequences. They show the location of the action points and provide the prerequisites for the corresponding tests for the EBC parameters.

The EBC parameter testing requires a test sequence, while power-on and power-off behaviour is controlled by the /RST signal.

Figure 31 defines the measuring EBC parameters - EBC signal chart.




**Key**

1 marker action point 1

2 marker action point 2

**Figure 31 — Measuring EBC parameters – EBC signal chart**

### 11.2.3 Measuring EBC parameters – Test sequences

#### 11.2.3.1 EBC test sequence #1 - off-state to on-state by /RST signal

Table 10 specifies the EBC test sequence #1, which checks the reset mechanism of the EBC and the minimal allowed time for the /RST signal to be set to logic 1 after the voltage provided by the power supply exceeds $V_T$.

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**Table 10 — EBC test sequence #1**

| Item | Content |
|---|---|
| Signal chart | Figure 31 |
| Initial state: inputs | $V_{EBC}$: according to operating conditions<br>/RST: logic 0<br>SP3: MOST50 bPHY stress pattern with nominal bit rate ($\rho_{BR}$) |
| Initial state: output | SP2: off-state |
| Test signal: inputs | /RST: logic 1 |
| Output/expected behaviour | The EBC transitions to on-state within time $t_{ON2}$(max.) after the /RST signal is set to logic 1. |

There are two aspects for treating this minimal allowed time.

The first is the power supply application aspect; the reset generator providing the signal shall be designed to ensure the /RST signal does not transition to logic 1 before $t_{D+}$(min.) time passes after the $V_{CCTX}$ measured on the EBC power supply pins crosses $V_T$.

The second is the EBC parameter aspect; ISO 21806-12:2021, Clause 10 mandates that when being supplied with an operating voltage within $V_{EBC_GR}$, the internal circuitry of the EBC settles into stable operation with the ability to perform transition detection within a time defined by the minimum value of the parameter $t_{D+}$. By driving the /RST signal to logic 1 at the $t_{D+}$(min.) time it is checked if the EBC complies to that specification.

Since there is no measurable marker that indicates when the EBC enters the on-state, an indirect method is used for testing the $t_{ON2}$(max.) conformance: after the maximum allowed time [end of $t_{ON2}$(max.) – marked as action point 1 in the EBC signal chart Figure 31], a check of on-state requirements is started.

For this test, along with the output power of the SP2 interface, also the SP2 signal quality is checked. At action point 1, the oscilloscope shall start capturing the data sequence, which is used for evaluating the SP2 signal quality.

To assist the capture of the SP2 data in on-state, the signal generator may assert the trigger signal to the oscilloscope $t_{ON2}$(max.) after activation of the test signal.

#### 11.2.3.2 EBC test sequence #2 – on-state to off-state by /RST signal

Table 11 specifies the EBC test sequence #2, which checks the reset mechanism of the EBC.

**Table 11 — EBC test sequence #2**

| Item | Content |
|---|---|
| Signal chart | Figure 31 |
| Initial state: inputs | $V_{EBC}$: according to operating conditions<br>/RST: logic 1<br>SP3: MOST50 bPHY stress pattern with nominal bit rate ($\rho_{BR}$) |
| Initial state: output | SP2: on-state |
| Test signal: inputs | /RST: logic 0 |
| Output/expected behaviour | The EBC transitions to off-state within time $t_{OFF2}$(max.) after the /RST signal is set to logic 0 and it stays in off-state as long as the /RST signal is set to logic 0. |

Since there is no measurable marker that indicates when the EBC enters the off-state, an indirect method is used: after the maximum allowed time [end of $t_{OFF2}$(max.) – marked as action point 2 in the EBC signal chart Figure 31], a check of off-state requirements is started.


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The oscilloscope shall start monitoring the SP2 output after the time marked as action point 2 to ensure the off-state requirement is met. A trigger signal from the signal generator is used to mark action point 2.

To trigger the oscilloscope, the signal generator may produce a signal marker $t_{OFF2}$(max.) time after switching the /RST signal to logic 0.

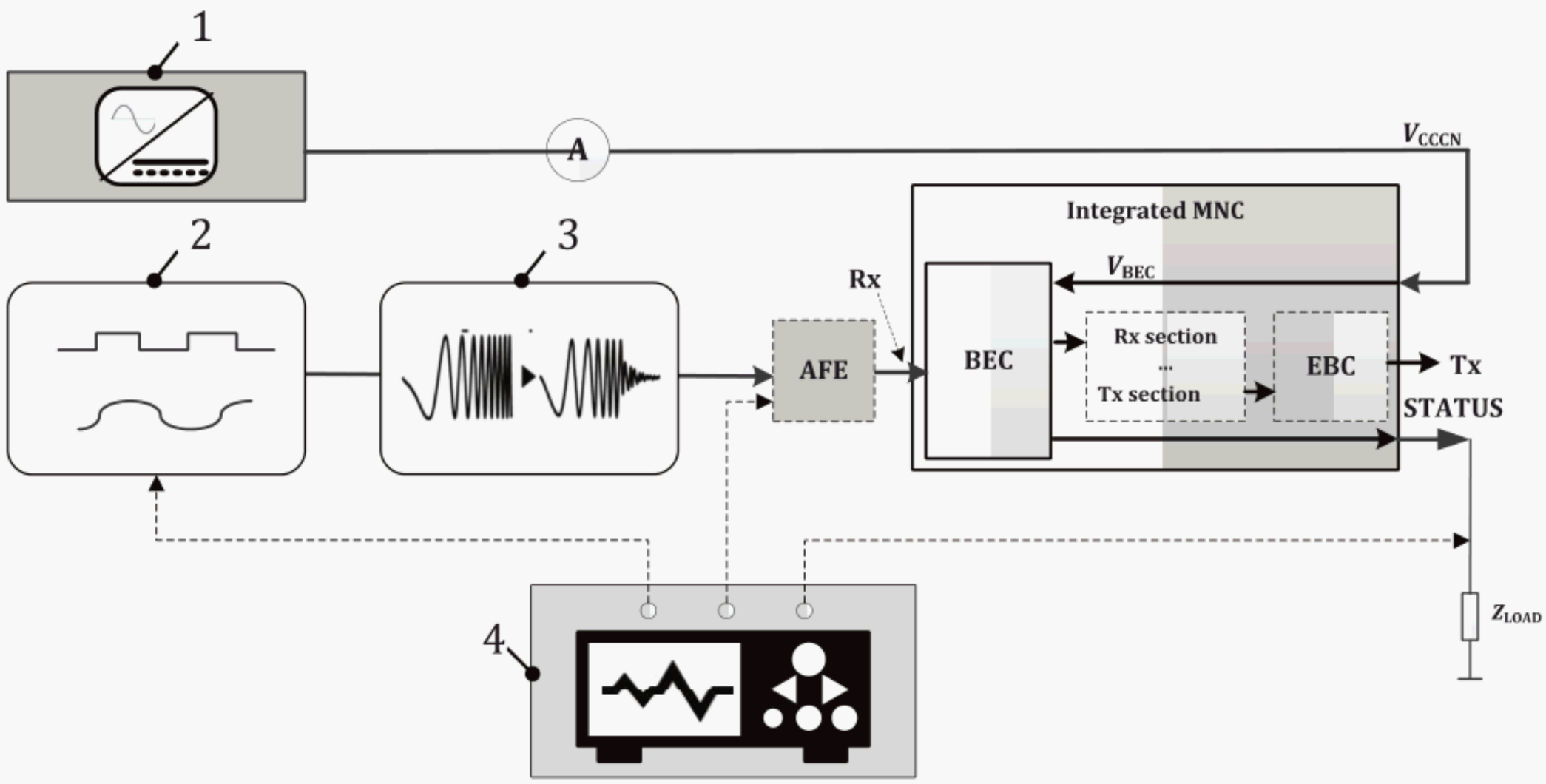
NOTE Long data set capture is preferred, since it is possible that the hold-off time that accompanies repetitive capture can lead to missed events.

## 11.3 Measuring BEC parameters

### 11.3.1 Measuring BEC parameters – Test set-up

ISO 21806-12 specifies a set of functional requirements and performance parameters for the BEC. Figure 32 and Figure 33 show examples of test set-ups for measuring BEC power-on and power-off parameters.

Set-up 1 is used to check the BEC response on an ECU. Stimulated events trigger STATUS responses, which can be measured. For functional verification, the resulting output signal can be forwarded to other nodes.




**Key**

1 programmable power supply
2 signal generator
3 cable assembly or its analogue representation
4 oscilloscope

**Figure 32 — Set-up 1 for measuring BEC power-on and power-off parameters**

Figure 33 shows the set-up 2, which is used to check the BEC response on chip level (MNC). Stimulation with arbitrary waveforms includes all relevant impairments.

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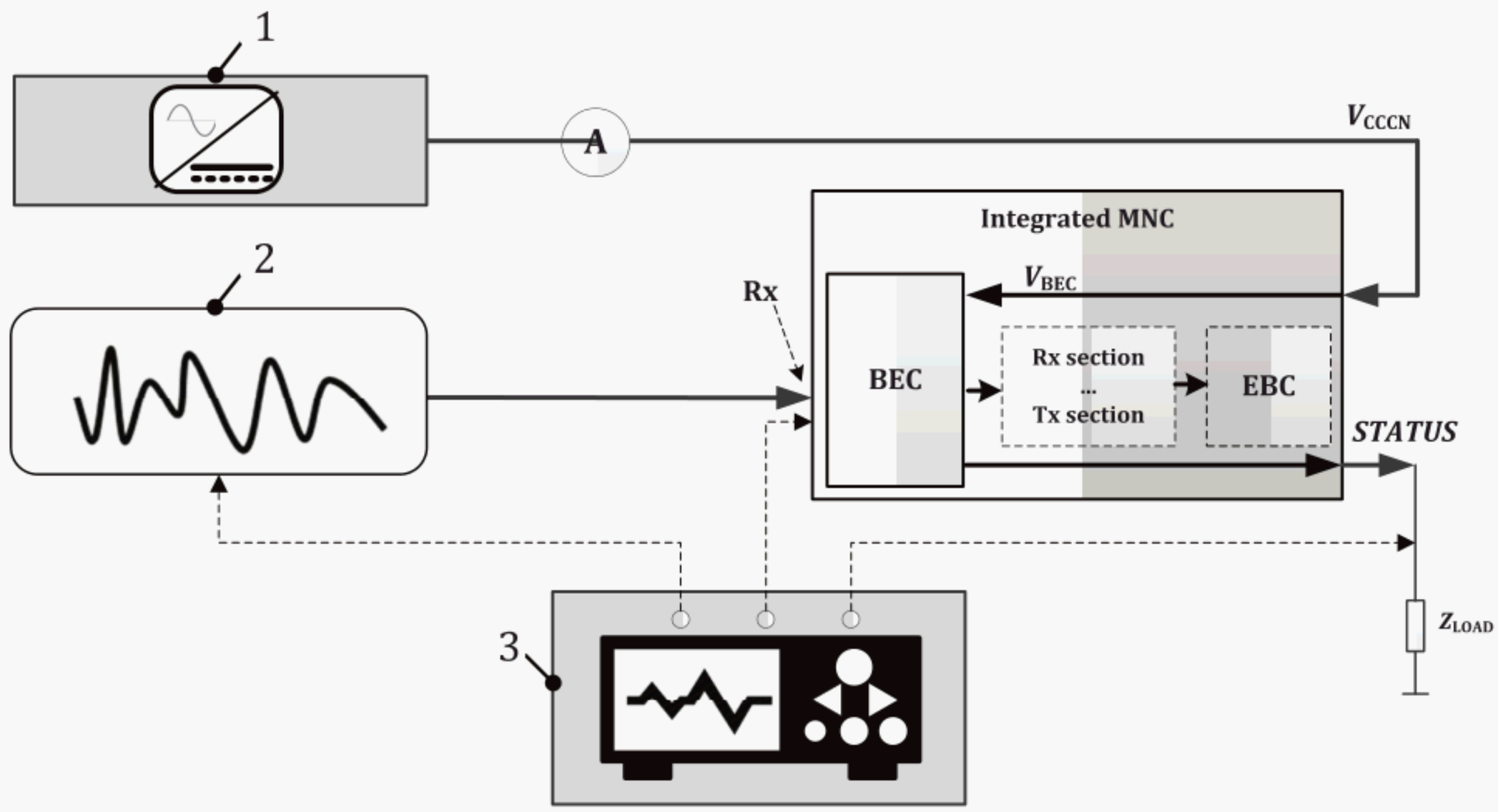


**Key**

1 programmable power supply

2 arbitrary signal generator

3 oscilloscope

**Figure 33 — Set-up 2 for measuring BEC power-on and power-off parameters**

The main parts of the set-ups (Figure 32 and Figure 33) are:

— the IUT is fitted according to the manufacturer's recommended set-up and is powered constantly during the test(s);

— response and timing are directly measured at the STATUS pin;

— functional verification can be realized by detecting Tx data at the MNC transmit terminal or an SP2 signal;

— the programmable power supply turns the BEC power on and off, and provides the desired supply voltage;

— a signal generator (i.e. pattern generator or arbitrary signal generator) or a test node is used to produce the stimuli (test patterns), followed by a cable assembly or an analogue cable representation; alternatively, an arbitrary signal generator is used;

— the oscilloscope captures input and output signal data;

— the ampere meter measures the current consumption of the BEC under test (in off-state).

The arbitrary signal generator shown in Figure 33 emulates the SP2 interface in a real network. Therefore, output signal amplitudes follow the specified values for SP2. In cases, where the cable emulation is already mathematically embedded in the arbitrary signal generator's output patterns, amplitude settings follow SP2 amplitude values and the targeted cable degradation.

As a general rule, the signal voltage amplitude at SP3 of the set-up emulates SP2 amplitudes and the targeted cable degradation. This is valid for the MOST50 bPHY stress pattern and for sine wave signals


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used for testing BEC power state requirements. The signal generator (Figure 32) and the cable or cable emulation also shall provide an off-state as defined for the EBC.

NOTE 1 BEC on-state and off-state depend on BEC power state requirements ($F_{ON}$, $F_{OFF}$) and signal voltage amplitude limits, which are specified in ISO 21806-12.

NOTE 2 The attenuation characteristic of the electrical interconnect (see 8.4) is a function of signal frequency and results in intersymbol interference. In consequence, short pulses of incoming data signals do not achieve full amplitude swing. Therefore, the BEC response on data patterns with strong attenuation is dominated by the shorter pulses. In order to stress this effect, the MOST50 bPHY stress pattern contains sub-pattern structures that address such corner cases sufficiently.

BEC power state requirements should be tested using pure sine wave signals.

Restrictions with respect to the STATUS signal may apply, see ISO 21806-12. In this case, the MNC supplier's instructions for testability are applicable.

### 11.3.2 Measuring BEC parameters – Signal chart

The signal chart represents the graphical view of the test sequence. It provides the prerequisites for the corresponding tests of the BEC parameters.

Figure 34 defines the measuring BEC parameters - BEC signal chart.

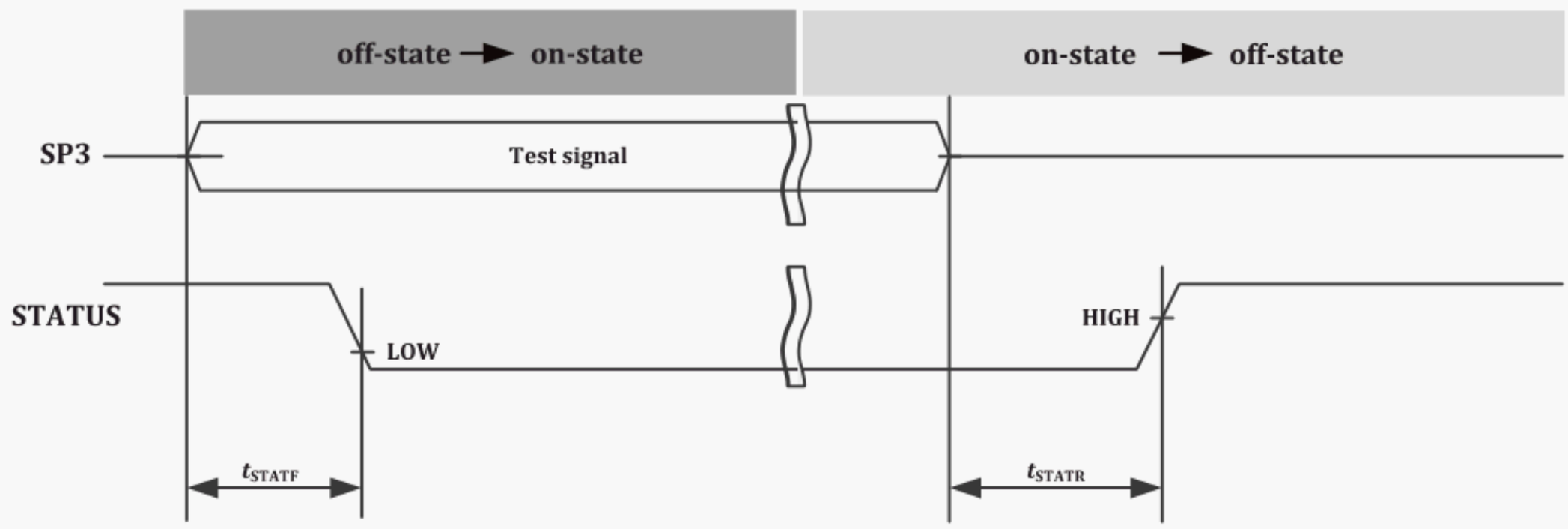


**Figure 34 — Measuring BEC parameters – BEC signal chart**

### 11.3.3 Measuring BEC parameters – Test sequences

#### 11.3.3.1 General

The test is performed according to the set-up described in 11.3.1.

The use of test signals with multiple test signal levels is recommended but at least the minimum and maximum values shall be used.

#### 11.3.3.2 BEC test sequence #1 – off-state to on-state

Table 12 specifies the BEC test sequence #1, which checks the wake-up mechanism of the BEC.

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**Table 12 — BEC test sequence #1**

| Item | Content |
|---|---|
| Signal chart | Figure 34 |
| Initial state: inputs | $V_{BEC}$: according to operating conditions<br>SP3: equivalent to SP2 (off-state) |
| Initial state: output | STATUS: logic 1 |
| Test signal: inputs | SP3: continuous sine wave within the range of $F_{OFF3}$ |
| Output/expected behaviour | The BEC remains in off-state with STATUS logic 1, being supplied with an input signal of a frequency within $F_{OFF3}$ requirements.<br>When no test signal is present, the BEC does not consume more than the sleep current, $I_{CCSLEEP}$(max.). During the test signal application, the BEC may consume more than $I_{CCSLEEP}$(max.). |

#### 11.3.3.3 BEC test sequence #2 – off-state to on-state

Table 13 specifies the BEC test sequence #2, which checks the wake-up mechanism of the BEC.

**Table 13 — BEC test sequence #2**

| Item | Content |
|---|---|
| Signal chart | Figure 34 |
| Initial state: inputs | $V_{BEC}$: according to operating conditions<br>SP3: equivalent to SP2 (off-state) |
| Initial state: output | STATUS: logic 1 |
| Test signal: inputs | SP3: continuous sine wave > $F_{ON3}$(min.)<br>signal voltage amplitude < $V_{OFF3}$ |
| Output/expected behaviour | The BEC remains in off-state with STATUS logic 1 being supplied with an input signal of a frequency greater than $F_{ON3}$ and an input signal with an amplitude of less than $V_{OFF3}$.<br>When no test signal is present, the BEC does not consume more than the sleep current, $I_{CCSLEEP}$(max.). During the test signal application, the BEC may consume more than $I_{CCSLEEP}$(max.). |

#### 11.3.3.4 BEC test sequence #3 – off-state to on-state

Table 14 specifies the BEC test sequence #3, which checks the transition detection and wake-up mechanism of the BEC.

**Table 14 — BEC test sequence #3**

| Item | Content |
|---|---|
| Signal chart | Figure 34 |
| Initial state: inputs | $V_{BEC}$: according to operating conditions<br>SP3: equivalent to SP2 (off-state) |
| Initial state: output | STATUS: logic 1; |
| Test signal: inputs | SP3: burst, sine wave > $F_{ON3}$(min.)<br>signal voltage amplitude > $V_{ON3_RMS}$<br>duration ≤ $t_{STATF}$(min.) |


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**Table 14** *(continued)*

| Item | Content |
|---|---|
| Output/expected behaviour | The BEC remains in off-state with STATUS logic 1 for at least $t_{STATF}$(min.) time, being supplied with an input signal of a frequency greater than $F_{ON3}$(min.) and an input signal with an amplitude of greater than $V_{ON3_RMS}$.<br>When no test signal is present, the BEC does not consume more than the sleep current, $I_{CCSLEEP}$(max.). During the test signal application, the BEC may consume more than $I_{CCSLEEP}$(max.). |

#### 11.3.3.5 BEC test sequence #4 – off-state to on-state

Table 15 specifies the BEC test sequence #4, which checks the transition detection and wake-up mechanism of the BEC.

**Table 15 — BEC test sequence #4**

| Item | Content | |
|---|---|---|
| Signal chart | Figure 34 | |
| Initial state: inputs | $V_{BEC}$:<br>SP3: | according to operating conditions<br>equivalent to SP2 (off-state) |
| Initial state: output | STATUS: | logic 1 |
| Test signal: inputs | SP3: | burst, sine wave > $F_{ON3}$(min.)<br>signal voltage amplitude > $V_{ON3_RMS}$<br>duration > $t_{STATF}$(min.) |
| Output/expected behaviour | The BEC transitions to on-state with STATUS logic 0 within $t_{STATF}$(min.) to $t_{STATF}$(max.). | |

#### 11.3.3.6 BEC test sequence #5 – on-state to off-state

Table 16 specifies the BEC test sequence #5, which checks the shutdown mechanism of the BEC.

**Table 16 — BEC test sequence #5**

| Item | Content | |
|---|---|---|
| Signal chart | Figure 34 | |
| Initial state: inputs | $V_{BEC}$:<br>SP3: | according to operating conditions<br>sine wave > $F_{ON3}$(min.)<br>signal voltage amplitude > $V_{ON3_RMS}$ |
| Initial state: output | STATUS: | logic 0 |
| Test signal: inputs | SP3: | signal voltage amplitude < $V_{OFF3}$ |
| Output/expected behaviour | The BEC transitions to off-state with STATUS logic 1 within $t_{STATR}$(max.).<br>Afterwards (no specified time), the BEC does not consume more than the sleep current $I_{CCSLEEP}$(max.). | |

#### 11.3.3.7 BEC test sequence #6 – off-state to on-state

Table 17 specifies the BEC test sequence #6, which checks the wake-up mechanism of the BEC.

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**Table 17 — BEC test sequence #6**

| Item | Content |
|---|---|
| Signal chart | Figure 34 |
| Initial state: inputs | $V_{BEC}$: according to operating conditions<br>SP3: MOST50 bPHY stress pattern with nominal $\rho_{BR}$<br>signal voltage amplitude < $V_{OFF3}$ |
| Initial state: output | STATUS: logic 1 |
| Test signal: inputs | SP3: signal voltage amplitude > $V_{ON3_RMS}$ |
| Output/expected behaviour | The BEC transitions to on-state with STATUS logic 0 within $t_{STATF}$(min.) to $t_{STATF}$(max.). |

### 11.3.3.8 BEC test sequence #7 – on-state to off-state

Table 18 specifies the BEC test sequence #7, which checks the shutdown mechanism of the BEC.

**Table 18 — BEC test sequence #7**

| Item | Content |
|---|---|
| Signal charts | Figure 34 |
| Initial state: inputs | $V_{BEC}$: according to operating conditions<br>SP3: MOST50 bPHY stress pattern with nominal $\rho_{BR}$<br>signal voltage amplitude > $V_{ON3_RMS}$ |
| Initial state: output | STATUS: logic 0 |
| Test signal: inputs | SP3: signal voltage amplitude < $V_{OFF3}$ |
| Output/expected behaviour | The BEC transitions to off-state with STATUS logic 1 within $t_{STATR}$(max.).<br>Afterwards (no specified time), the BEC does not consume more than the sleep current $I_{CCSLEEP}$(max.). |

## 12 Detecting bit rate (frequency reference)

The bit rate is detected as follows.

— Data pulses range from 2 UI to 6 UI yielding five different pulse widths (2 UI, 3 UI, 4 UI, 5 UI, and 6 UI). A clock at UI rate represents a cycle time of 1 UI, which is twice the bit rate (i.e. for a $\rho_{Fs}$ of 48 kHz, the bit rate is 49,152 Mbit/s and the UI clock is 98,304 MHz).

— A method of extracting the UI clock out of a waveform is a mandatory function to be provided with the oscilloscope. In a first step, the recovered UI clock is a linear approximation that fits best to the acquired waveform in terms of phase and frequency. The approximation of the clock's phase shall be performed with regard to the rising edges of the data stream only. Then the bit rate is half the UI rate.

— The bit rate can be measured with the MOST50 bPHY stress pattern or any other valid data pattern. Set-up of the oscilloscope shall follow the general requirements (see 6.2) using acquisition length of 10 megasample and a sampling rate of 5 gigasample/s.


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# 13 System performance

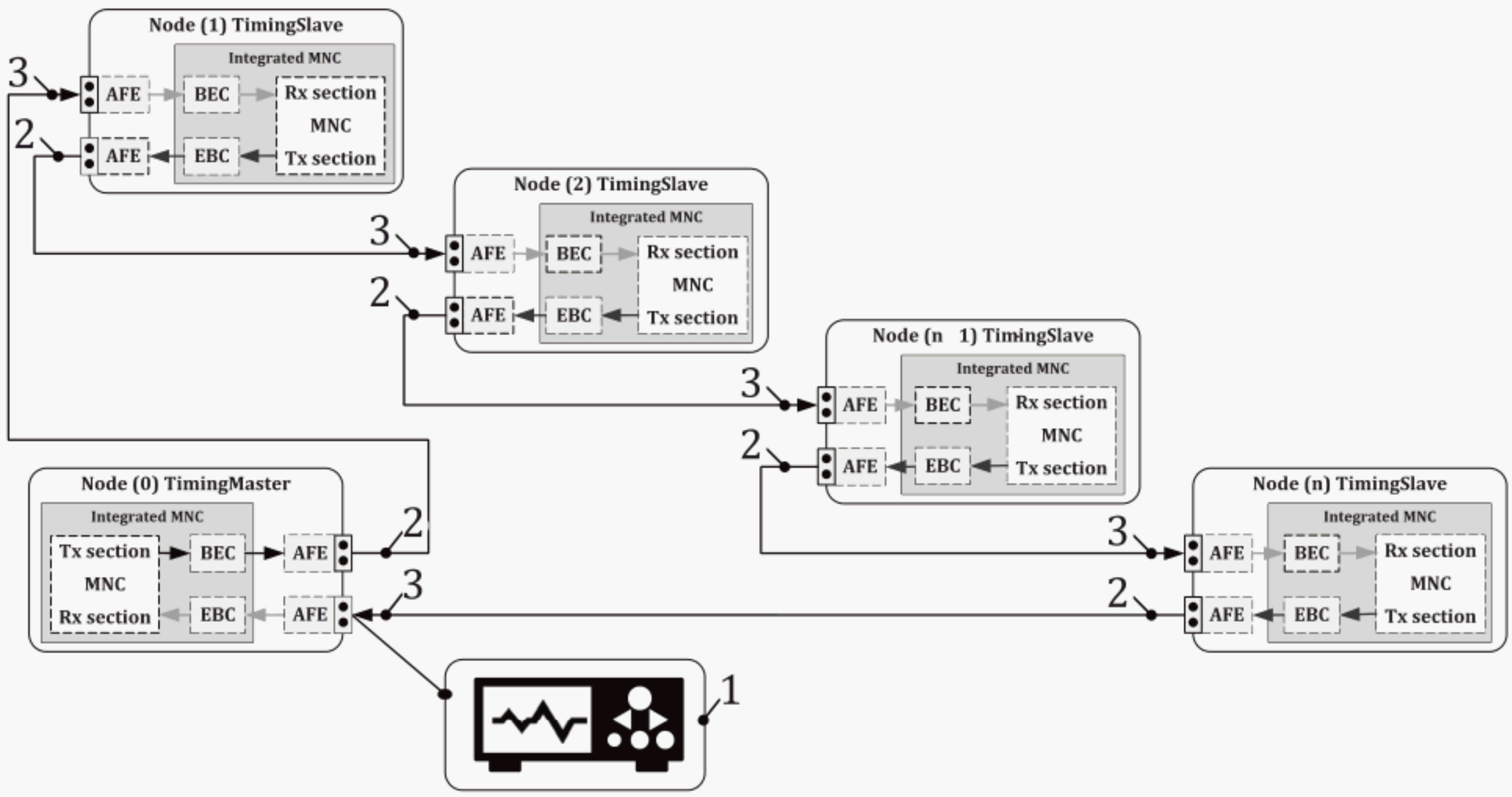
## 13.1 General

The system-level specifications apply to an entire MOST network.

## 13.2 SP3 receiver tolerance

Unlike the link-level tests, which use a pattern generator as the signal source, the system-level tests use live data from a MOST50 network. Using the eye diagram methodologies described in Clause 9, a measurement is taken at SP3 of the TimingMaster node. By taking the measurement in this way, one can quantify the total jitter accumulation in the network. This measurement is applicable for every node in the network at SP3.

Figure 35 shows the SP3 receiver tolerance set-up.




**Key**

1 oscilloscope

2 SP2

3 SP3

**Figure 35 — SP3 receiver tolerance set-up**

## 13.3 TimingMaster delay tolerance

TimingMaster delay tolerance is a measure of end-to-end delay and phase variation between SP2 and SP3 of the MOST device that contains the TimingMaster. To ensure proper network operation, the total network delay shall not exceed the specified maximum (see ISO 21806-12:2021, 11.2).

Following the set-up diagram shown in Figure 36, the total delay can be measured with an oscilloscope.

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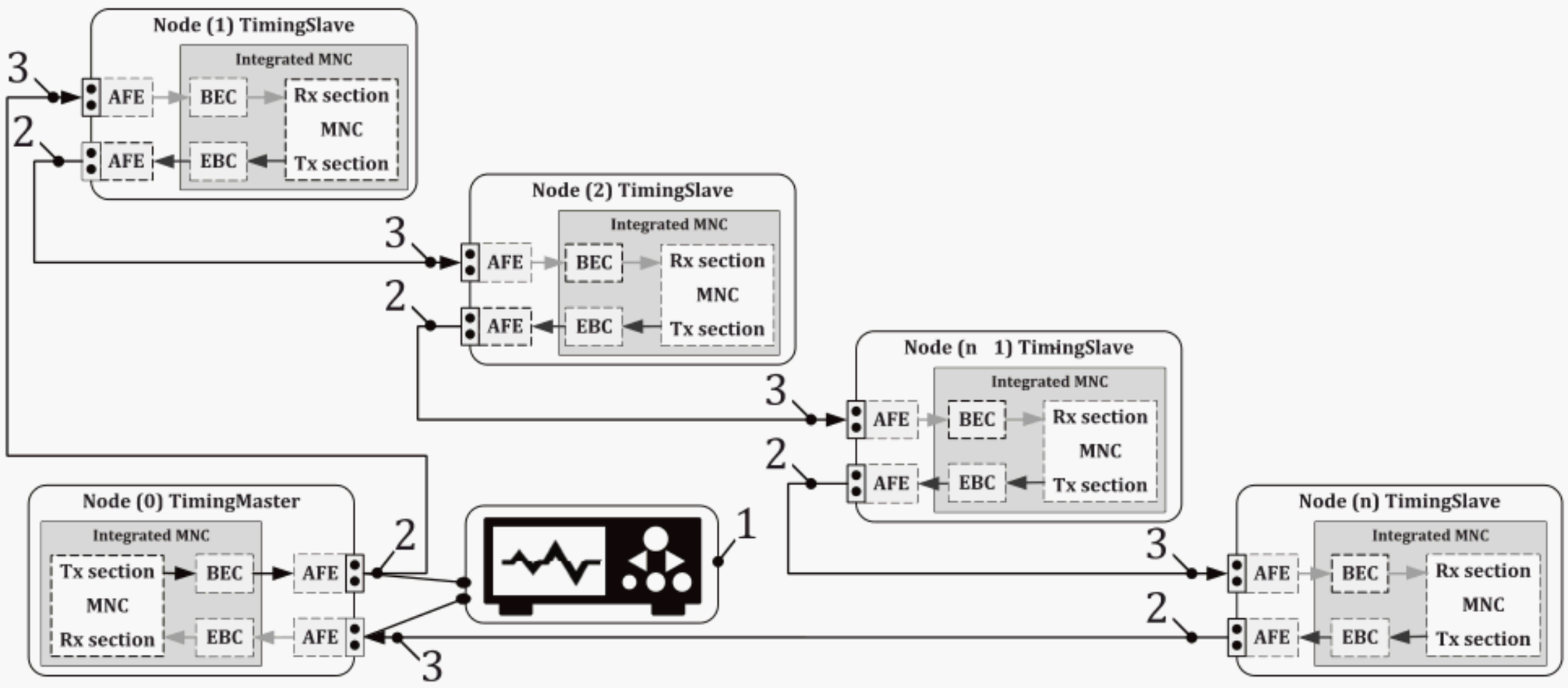


**Key**

1 oscilloscope

2 SP2

3 SP3

**Figure 36 — TimingMaster delay tolerance set-up**

Table 19 specifies the procedure used to measure the total delay. The oscilloscope used shall be able to trigger on a specified period and shall have software functions for tracking periods. Two differential probes are needed.

**Table 19 — TimingMaster delay measurement procedure**

| Action | Description |
|---|---|
| Acquire a waveform | For this measurement, the sampling memory of the oscilloscope should be adjusted to capture at least one frame of data. One differential probe is connected to SP2 of the TimingMaster node. A second differential probe is connected to SP3 of the TimingMaster node. The vertical scale is adjusted to achieve sufficient vertical resolution on both channels.<br>The trigger settings are adjusted to trigger on the interval of rising edges (period) on SP2. The interval should be set to 10 UI ± 0,5 UI. The trigger mode should be normal.<br>A sequence of the data stream ("waveform") is sampled into the oscilloscope's memory. |
| Measure the period | The MOST50 data stream contains a period of 10 UI at the start of each frame. This long period can be used as a marker to measure the delay between any two points in the network.<br>Configure the oscilloscope to measure the period of both SP2 and SP3. |
| Track the period | Configure the oscilloscope to display a "track" waveform for both SP2 and SP3 period measurements. This should result in two waveforms (see Figure 37 and Figure 38) with time on the y-axis where the line indicates the length of the current period. |
| Measure the delay | Configure the oscilloscope display to show only the SP2 and SP3 period tracks. Turn on infinite persistence and adjust the display to show the 10 UI segment for both SP3 and SP3.<br>Using the cursor, measure the total time between the trigger point and the rightmost edge of the SP3 10 UI period. This is the TimingMaster delay. |

Figure 37 shows an example of tracking the SP3 period.


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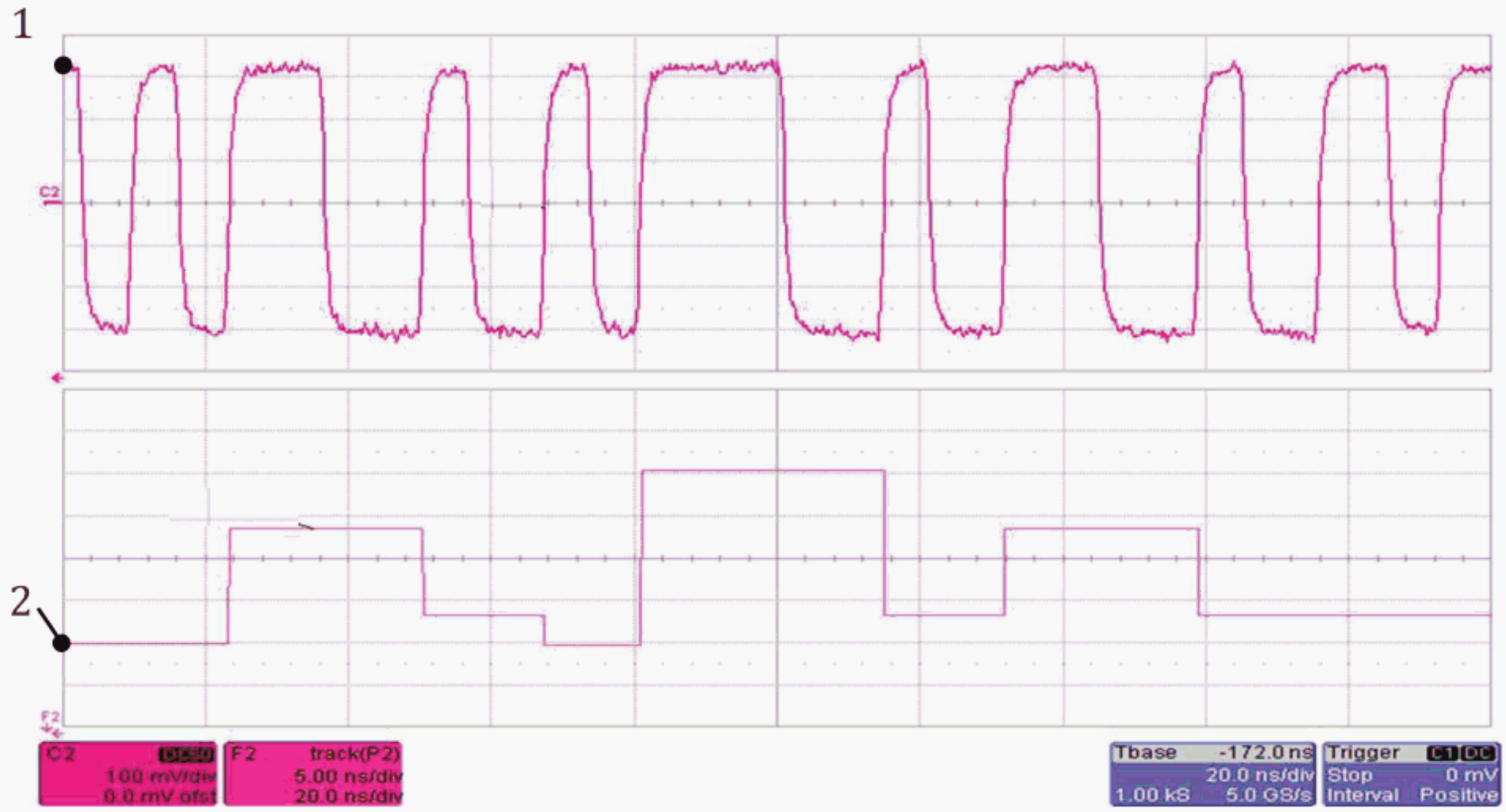


**Key**

1 acquired data signal at SP3

2 measured period at SP3

**Figure 37 — Example of tracking the SP3 period**

Figure 38 shows how the TimingMaster delay is measured.

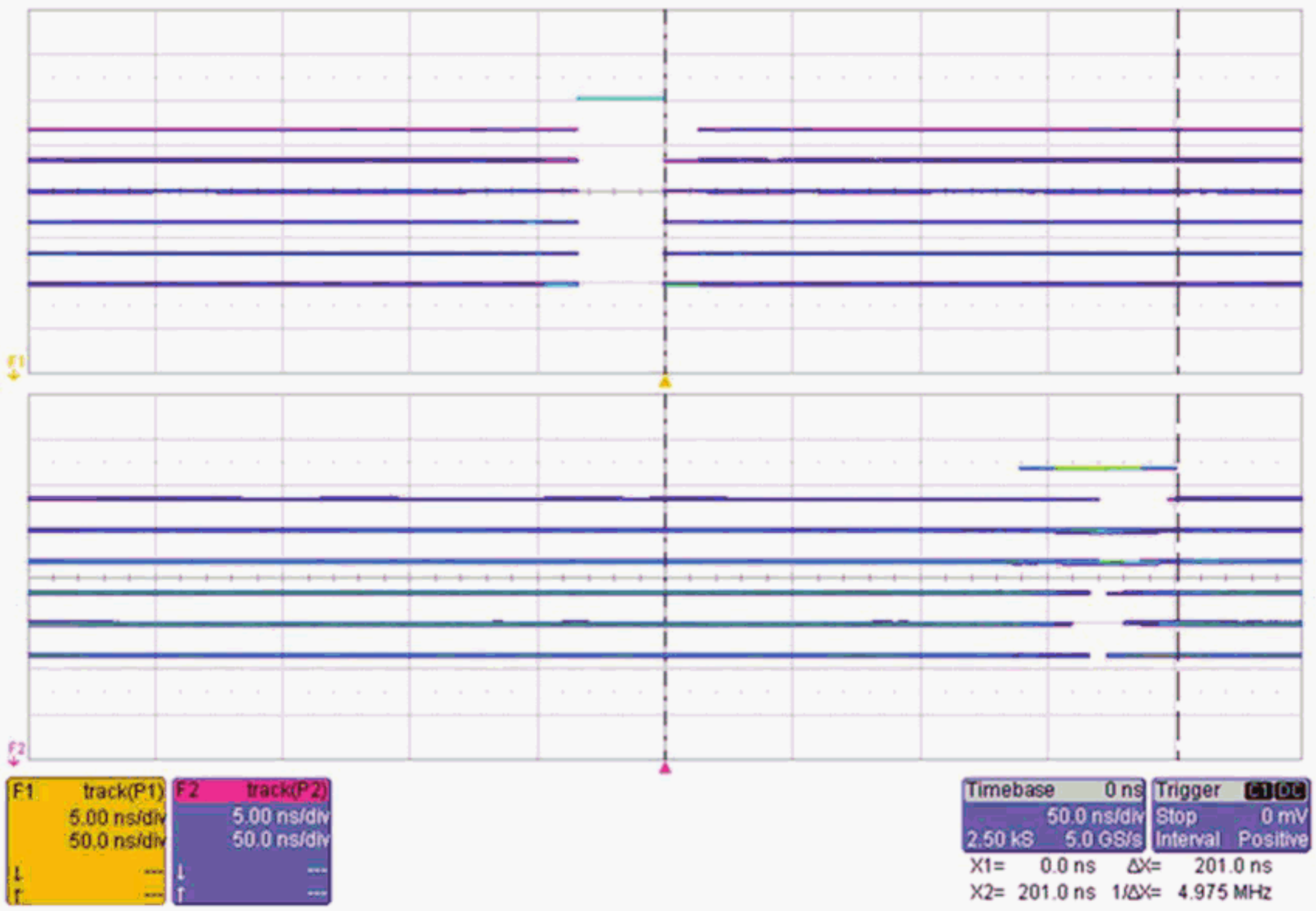


**Figure 38 — TimingMaster delay**

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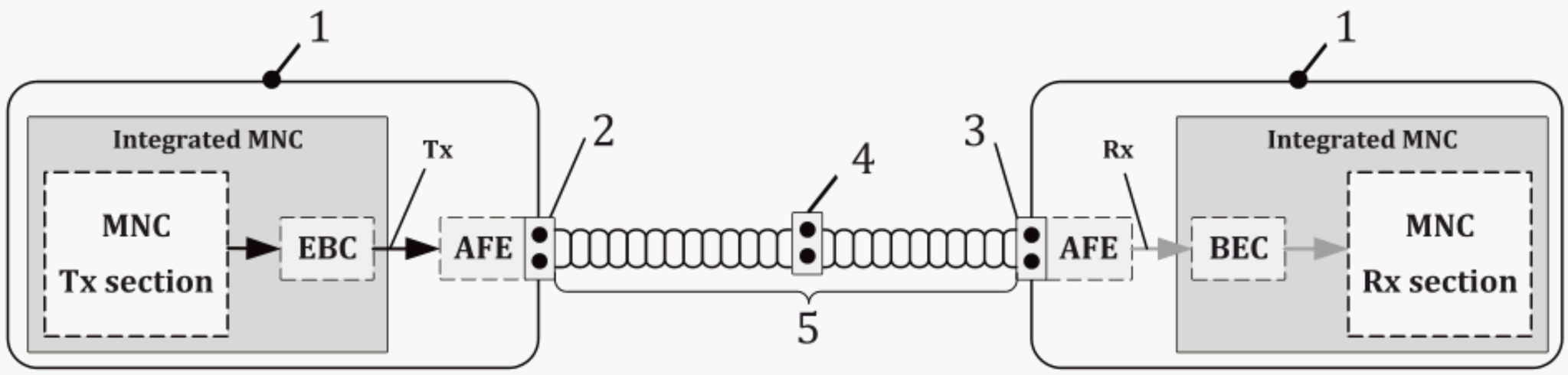
# 14 Conformance test of 50-Mbit/s balanced media physical layer

## 14.1 Location of interfaces

SP2 describes input parameters of an ECU's output signal. Performance criteria for SP2 include EBC and AFE impact on signal quality.

SP3 describes the minimum signal quality requirements at the ECU's input interface. The stimulus signal for SP3 can be composed by combination of worst-case SP2 performance and deterioration due to channel impairment.

Figure 39 shows the SP locations.




**Key**

1 MOST device
2 SP2
3 SP3
4 in-line connectors
5 channel, balanced media

**Figure 39 — SP locations**

Signals that fulfil the SP3 parameters can be recovered by the MNC. Signals outside the ranges might cause bit errors. On the transmit terminal (Tx) of the MNC of the following node, a recovered signal is available according to SP2 requirements, and timing distortion (except transferred jitter) is eliminated.

## 14.2 Control signals

In addition to power supply terminals and data pins, an EBC provides an /RST input. The EBC provides activity detection in order to enable/disable MOST output. Activity depends on the $V_{\mathrm{EBC}}$ state, the data content at the input of the EBC, and the /RST input.

The BEC also provides activity detection. Depending on the characteristics of the input signal (power level, signal content), on-state/off-state is signalled by the STATUS pin.

Figure 40 shows the control signals for power-on and power-off behaviour.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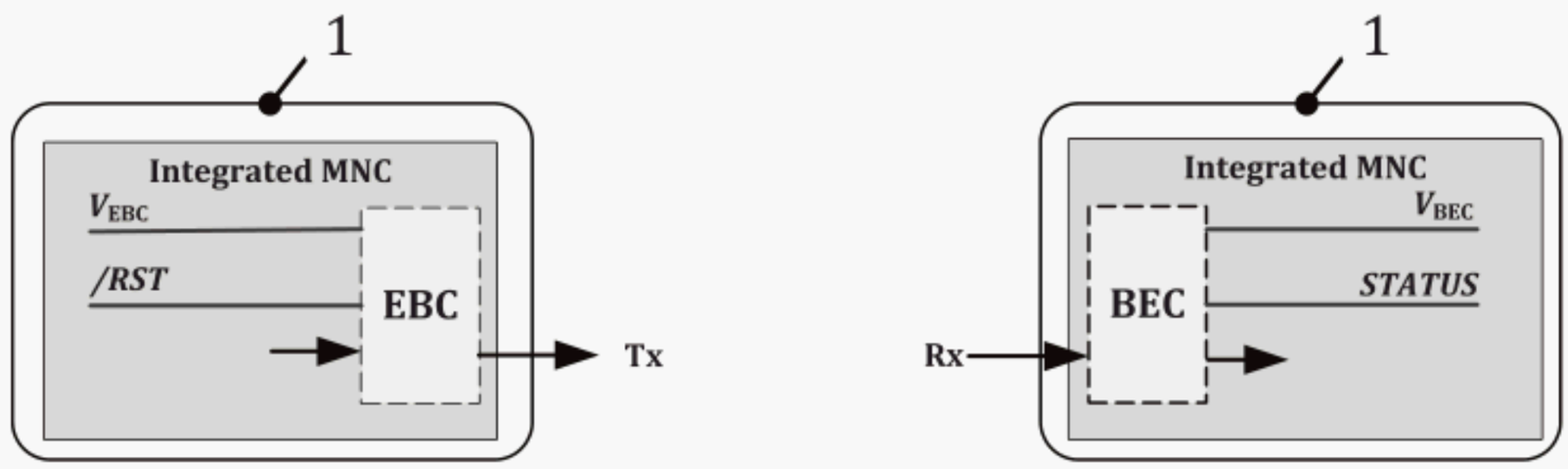


**Key**

1 MOST device

**Figure 40 — Control signals for power-on and power-off behaviour**

## 14.3 Limited access to specification points

On MOST device level, measurement has no access to the transmit terminal (Tx) and the receive terminal (Rx). Therefore, variation on input parameters can only be applied at SP3. Parameters can only be measured at SP2. The power supply of MNC, EBC, and BEC is fixed by the design of the device and cannot be varied. Considering these circumstances, the limited physical layer conformance specifies a simplified test procedure that uses only the accessible interfaces of a MOST device, SP2 and SP3 (see Clause 15).

## 14.4 Parameter overview

Table 20 specifies the conformance procedures for the parameters of ISO 21806-12 that are relevant for physical layer conformance. For each parameter, it indicates how conformance can be achieved, depending on the type: MOST component (EBC/BEC), MOST module, or MOST device.

NOTE Developers of MOST components or MOST modules ensure that their products fulfil the specification under minimum/maximum conditions of their input parameters, considering environmental conditions and lifetime. The verification of these parameters is done using the procedure of the product characterization.

**Table 20 — Conformance procedures for all parameters of specification points of MOST devices**

| SP | Parameter | Conformance procedure |
|---|---|---|
| SP2 | Signal voltage amplitude $V_{RMS}$ | M[a] ($T$, $U$) |
| | Alignment jitter according to eye mask | M[a] ($T$, $U$) |
| | Transferred jitter (RMS) | M[a] ($T$, $U$) |
| | RL of ECU interface | M[a] ($T_{Typ}$) |
| SP3 | Limited physical layer test of data consistency | C[b] ($T$, $U$, $A$) |
| | RL of ECU interface | M[a] ($T_{Typ}$) |

[a] Measure ($T$ = temperature range, $T_{Typ}$ = typical temperature, $U$ = voltage range, $A$ = attenuation).

[b] Sample check ($T$ = temperature range, $U$ = voltage range, $A$ = attenuation); check for bit errors by using methods and indicators as defined in FBlock EnhancedTestability or FBlock ExtendedNetworkControl.

The conformance verification of development tools is described in Annex A. The status of Annex A is informative.

# 15 Limited physical layer conformance

## 15.1 Overview

Limited physical layer conformance refers to MOST devices (see 14.3).

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An overview of the parameters to be tested and verified is shown in Table 20.

## 15.2 Test set-up

Figure 41 specifies the test set-up for limited physical layer verification comprising the following equipment:

— LT (tester node): TimingMaster/TimingSlave, pattern generation;

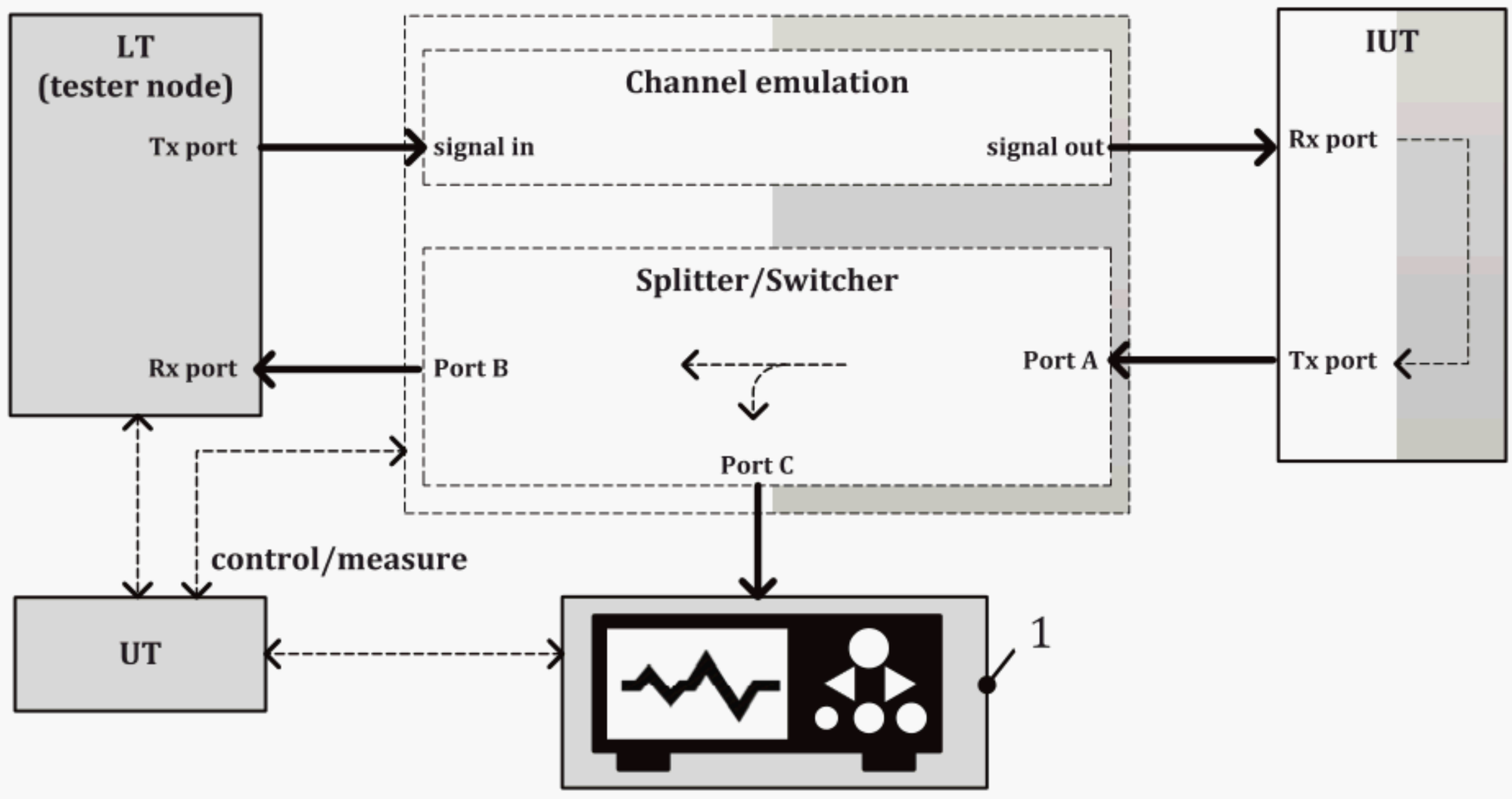
— channel emulation: cable or analogue filters representing channel losses;

— splitter/switcher: 3-port device that provides a replica of the analogue Port A signal for Port C and a digital representation of the SP2 signal for Port B;

— oscilloscope;

— UT: receive quality check;

— IUT.




**Key**

1 oscilloscope

**Figure 41 — Test set-up for limited physical layer conformance test**

The following is a list of purposes of the test set-up.

— Proof of valid data transmission in presence of various stress scenarios applied to the receive path of the IUT.

— Sample check of lock condition and data error state, acquired by the IUT's receive section.

— Check of lock condition and data error state, acquired by the tester node receive section.

— Test of signal integrity of IUT's signal at SP2.

— Test of signal integrity includes measurement of signal voltage amplitude RMS, PSD, and timing. The test flow shown in 15.5 requires a closed loop between the tester node and the IUT, providing communication over MOST.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— Functional test of wake-up and shutdown.

## 15.3 Generating test signals for the IUT input section SP3

A test signal for testing the IUT's input section may be varied in several instances and combinations of these instances (e.g. timing properties, pulse shape characteristics, data content, and interconnect attenuation). A subset of such variations is realized with the tester node and the channel emulation, which is a mandatory tool for limited physical layer conformance test.

The UT initiates and controls the test sequences. The tester node controls the IUT using communication via the MOST control channel. It addresses the IUT's FBlock EnhancedTestability or FBlock ExtendedNetworkControl, which cover all necessary IUT functions for the tests (e.g., retimed bypass mode, handling of various error counters). The tester node is capable of acting as TimingMaster or TimingSlave. Besides MOST communication, the tester node has the capability to send the MOST50 bPHY stress pattern.

For the test, the MOST50 bPHY stress pattern signal is attenuated and bandwidth-limited due to the transport medium before being applied to the IUT's SP3 interface.

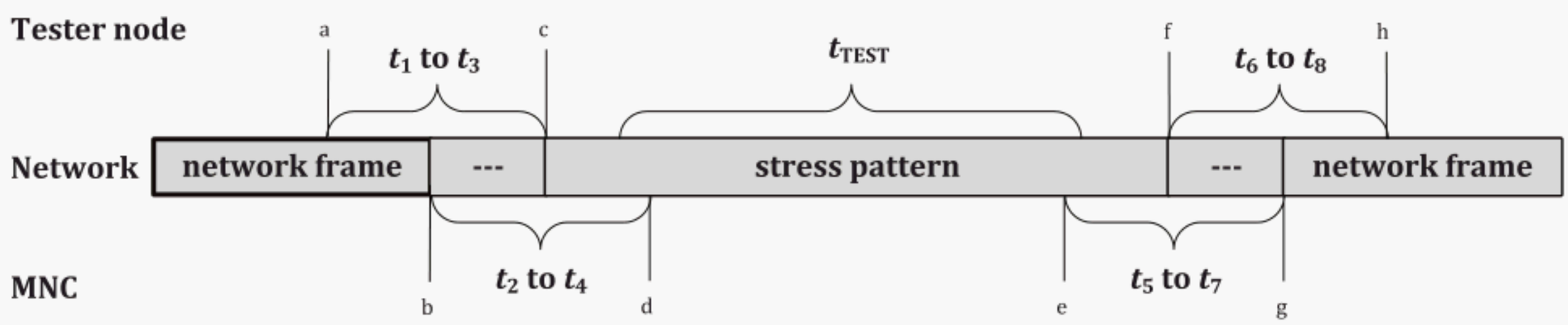
## 15.4 Analysis of test results

Error counters are implemented in the IUT (FBlock EnhancedTestability or FBlock ExtendedNetworkControl). These counters give a measure for communication errors on the input of a MOST device. These counters are activated during the test sequence. The tester node shall read the counter values after the test.

During the test sequence, the IUT is set to retimed bypass mode. This means that the recovered data on the input side is sampled with the internal clock and transferred to the output. Therefore, as long as there are no bit errors, the MOST50 bPHY stress pattern created by the tester node appears with identical content on the output of the IUT.

## 15.5 Test flow overview

Figure 42 shows the test flow overview.




**Key**

a $t_1$: the tester node sends a command to the IUT over MOST (FBlock ExtendedNetworkControl) to enter test mode.

b $t_2$: the IUT enters retimed bypass mode.

c $t_3$: the tester node starts transmitting the MOST50 bPHY stress pattern.

d $t_4$: IUT clears the error counter and the lock log.

e $t_5$: IUT reads the error counter and the lock log.

f $t_6$: the tester node instructs the IUT to switch off the retimed bypass.

g $t_7$: the IUT switches off the retimed bypass.

h $t_8$: the tester node reads the result.

**Figure 42 — Test flow overview**

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Switching times ($t_1$ to $t_3$, $t_2$ to $t_4$, $t_5$ to $t_7$, and $t_6$ to $t_8$) shall be in the range of 10 ms to 500 ms with accuracy ≤10 ms.

Lead-in/lead-out shall be in the range of 500 ms to 2 000 ms (typical: 1 000 ms).

$t_{TEST}$ time shall be in the range 1 s to 1 000 s with accuracy ≤ 10 ms.

The maximum duration shall be 1 000 s.

Test of multi-node MOST devices with two MNCs:

— test set-up:

  The test set-up shown in Figure 41 shall be used. The IUT consists of SP3 of MNC 1 and SP2 of MNC2. MNC 1 is connected to MNC 2, which provides the SP2 output.

— procedure:

  MNC 2 (node position address $402_{16}$) shall be set to retimed bypass mode with the value of duration of 1 000 s. Then MNC 1 (node position address $401_{16}$) shall be set to retimed bypass mode. The result provided by the FBlock EnhancedTestability or the FBlock ExtendedNetworkControl is read by the tester node, using the node position address $401_{16}$.

  NOTE The observed pattern is inverted.

## 15.6 Measurement of SP3 input signal of the IUT

In order to create stress scenarios for the IUT's SP3 interface, the cable emulation is varied, which influences frequency spectrum and signal strength at SP3:

— low attenuation cable;

— medium attenuation cable;

— maximum attenuation cable (worst case according to ISO 21806-12).

The stress conditions for cable emulation shall be in accordance with Annex B. The status of Annex B is normative.

The following requirements apply to the output signal of the tester node:

— the test set-up shall fulfil all parameters for SP3 as specified in ISO 21806-12;

— the MOST50 bPHY stress pattern as specified in ISO 21806-12 shall be applied.

Table 21 shows the summary of test cases.

**Table 21 — Summary of test cases**

| Test case | Attenuation cable | Temperature and voltage range |
|---|---|---|
| 1 | Low attenuation cable | $T_{23\,°C}$ and $U_{typ}$ |
| 2 | Medium attenuation cable | $T_{23\,°C}$ and $U_{typ}$ |
| 3 | Maximum attenuation cable | $T_{23\,°C}$ and $U_{typ}$ |
| 4 | Low attenuation cable | $T_{max}$ and $U_{min}$ |
| 5 | Medium attenuation cable | $T_{max}$ and $U_{min}$ |
| 6 | Maximum attenuation cable | $T_{max}$ and $U_{min}$ |
| 7 | Low attenuation cable | $T_{max}$ and $U_{max}$ |
| 8 | Medium attenuation cable | $T_{max}$ and $U_{max}$ |
| 9 | Maximum attenuation cable | $T_{max}$ and $U_{max}$ |


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**Table 21** *(continued)*

| Test case | Attenuation cable | Temperature and voltage range |
|---|---|---|
| 10 | Low attenuation cable | $T_{min}$ and $U_{min}$ |
| 11 | Medium attenuation cable | $T_{min}$ and $U_{min}$ |
| 12 | Maximum attenuation cable | $T_{min}$ and $U_{min}$ |
| 13 | Low attenuation cable | $T_{min}$ and $U_{max}$ |
| 14 | Medium attenuation cable | $T_{min}$ and $U_{max}$ |
| 15 | Maximum attenuation cable | $T_{min}$ and $U_{max}$ |

## 15.7 Measurement of SP2 output signal of the IUT

According to Table 20, the parameters in Table 22 shall be measured for each test case. The tests shall be performed in the following sequence:

a) $T_{23\,°C}$ and $U_{typ}$;

b) $T_{min}$ and $U_{min}$;

c) $T_{min}$ and $U_{max}$;

d) $T_{max}$ and $U_{min}$;

e) $T_{max}$ and $U_{max}$.

Table 22 specifies the stimulus for the measurements at SP2 of the IUT.

**Table 22 — Stimulus for the measurements at SP2 of the IUT**

| Measurement of the SP2 signal | Stimulus |
|---|---|
| Signal voltage amplitude $V_{RMS2}$ | MOST50 bPHY stress pattern |
| PSD | MOST50 bPHY PSD pattern |
| Transferred jitter, $J_{tr2}$ | MOST50 bPHY stress pattern |
| Alignment jitter | MOST50 bPHY stress pattern |

## 15.8 Measurement of RL

The RL of the ECU interfaces SP2 and SP3 is measured at the ECU's device connector.

For set-up, EN 50289-1-11 shall be followed.

RL at SP2 and RL at SP3 describe impedance matching considering all relevant components. This includes passive components in the AFE as well as active components inside the MNC or passive components inside the MNC activated by MNC functionality.

## 15.9 Functional test of wake-up and shutdown

For verification of physical layer MOST components within MOST devices, wake-up and shutdown behaviour shall be tested using the test set-up. The tester node is the TimingMaster or a TimingSlave, depending on the IUT.

a) Wake-up:

Initially, the IUT is in `s_NetInterface_Sleep` (detectable by monitoring of power consumption). The tester node switches on its MOST output to create a wake-up event for the IUT. Subsequently, the IUT switches on its MOST output.

The test is only feasible for an IUT that can be woken up by network activity.

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b) Shutdown:

1) If the IUT is a TimingSlave, the tester node shall set the shutdown flag ($t_0$) and shall switch off the MOST output ($t_1$).

Expected result: the IUT switches off the MOST output.

If the IUT is the TimingMaster, the tester node shall switch off the MOST output ($t_1$). The IUT detects that the shutdown flag is not set.

Expected result: the IUT sets the shutdown flag and switches off the MOST output.

## 16 Direct physical measuring accuracy

The following parameters are relevant for measurement equipment:

— requested accuracy;

— validated measurement uncertainty (95 % confidence interval);

— systematic measurement deviation (either negligible or to be compensated).

Table 23 specifies the accuracy of the measurement set-up.

**Table 23 — Accuracy of measurement set-up**

| Item | Direct physical measuring accuracy |
|---|---|
| Operating voltage of IUT | ±0,25 V range for limited conformance; |
| $V_{RMS}$ signal amplitude | ±7 mV steady state amplitude; |
| Timing | — alignment jitter according to eye mask:<br>— alignment jitter according to eye mask measurement is a pass/fail test.<br>— ±7 mV steady state amplitude;<br>— ±50 ps.<br>— transferred jitter: ±10 ps. |
| Attenuation and RL | ±0,9 dB |
| Temperature | ±2 °C |


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# Annex A
(informative)

# Limited physical layer conformance for development tools

The example test plan for a data logger (development tool) is shown in Table A.1. In this example, due to a missing FBlock EnhancedTestability, the data consistency cannot be tested during limited physical layer conformance and is marked "not tested".

**Table A.1 — Example test plan for a data logger**

| Parameter | Result |
|---|---|
| Unlock (FBlock EnhancedTestability lock status) | not tested |
| Bit error (FBlock EnhancedTestability error counter value) | not tested |
| Unlock (tester node) | not tested |
| Bit error (tester node) | not tested |
| $V_{RMS}$ signal amplitude | passed |
| Transfer jitter | passed |
| Alignment jitter | passed |
| Functional wake-up | passed |
| Functional shutdown | passed |
| RL (SP2 and SP3) | passed |
| Limited physical layer test of data consistency | not tested |

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# Annex B
(normative)

# SP3 stress conditions

Table B.1 specifies the cable models for the SP3 stress conditions.

**Table B.1 — Cable models**

| Cable model | Attenuation at 10 MHz | Attenuation at 33 MHz |
|---|---|---|
| Low | 0 dB down to -1 dB | 0 dB down to -1 dB |
| Medium | -1 dB down to -2 dB | -2 dB down to -3 dB |
| Maximum | -2 dB down to -2,6 dB | -3,9 dB down to -4,9 dB |


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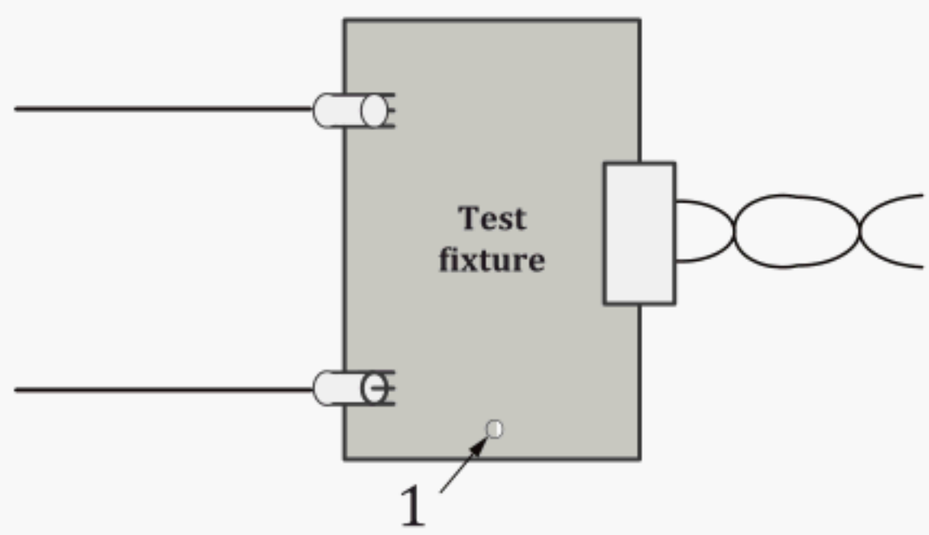
# Annex C
(informative)

# Test fixture

Figure C.1 shows the test fixture for interfacing measurement equipment with an IUT.

Test fixtures are required when connecting differential signal terminals of components or modules under test to the respective measurement equipment.




**Key**

1 fixture ground

**Figure C.1 — Test fixture**

Examples are:

— signal quality evaluation with an oscilloscope using two single ended channels and oscilloscope's internal 50 Ω termination;

— measurement of attenuation using a VNA;

— measurement of RL using a VNA.

IUTs (e.g. SP2 of a MOST device or electrical interconnect) provide an interface with differential signal structure and a pair of customer defined contact geometries. Measurement equipment is being attached using single ended interfaces with SubMiniature version A (SMA) connectors (or similar RF laboratory connectors).

As ISO 21806-12 does not specify a particular connector system, no unique test fixture is defined but the following recommendations are provided:

— the test fixture should have a low insertion loss;

— the test fixture should be highly symmetrical between the two wires of the pair;

— the test fixture should be well adapted to the single-ended impedance of the measuring instrument (50 Ω).

Two versions of the test fixture exist:

— test fixture with connector jacks to interface with an ECU (see Figure C.2). Here, the jacks should be extended to provide contact with the ECU side pin header;

— test fixture with male contacts to interface with harness side female connectors (see Figure C.3). The pins at the fixture should be extended to provide contact with a female header.

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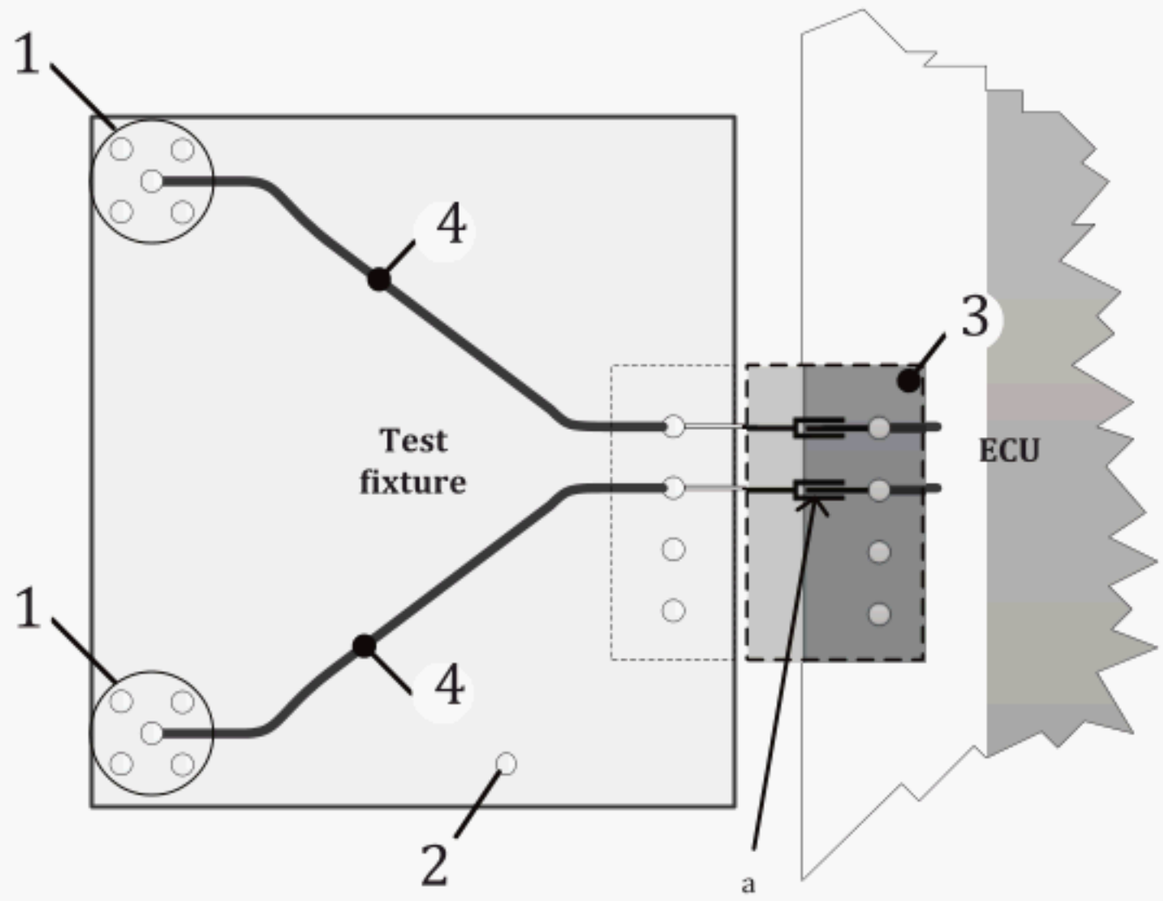
Figure C.2 shows the test fixture for connecting ECU.




**Key**

1 lab equipment connector (SMA)

2 fixture ground

3 ECU connector (e.g. MQS)

4 50 Ω single ended line

a Extended connector jacks required to interface with pins on ECU connector.

**Figure C.2 — Test fixture for connecting ECU**

Figure C.3 shows the test fixture for connecting a wire harness.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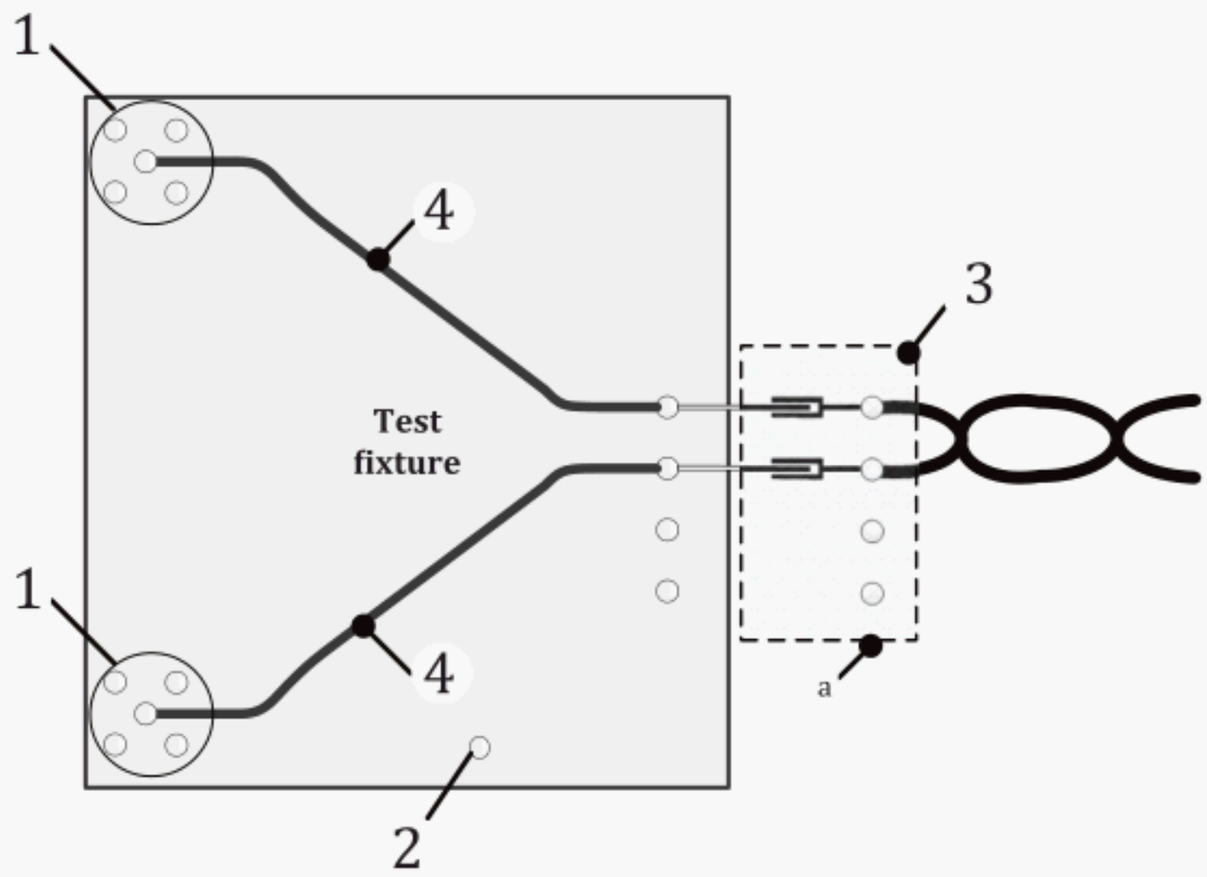


**Key**

1 lab equipment connector (SMA)

2 fixture ground

3 harness connector (e.g. MQS)

4 50 Ω single ended line

a Extended connector pins required to interface with jacks on wire-harness connector.

**Figure C.3 — Test fixture for connecting wire harness**

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# Annex D
(informative)

# Overview on test modes

Table D.1 lists test modes required to measure parameters as specified in Reference [2].

**Table D.1 — Overview on test modes**

| Test mode | Test case | Condition |
|---|---|---|
| MOST50 bPHY stress pattern | SP2 link quality:<br>— signal voltage amplitude $V_{RMS2}$;<br>— alignment jitter, according to eye mask $A_2$ to $D_2$;<br>— transferred jitter $J_{tr2}$. | Data signal at SP2 provides data content as specified for MOST50 bPHY stress pattern. |
| MOST50 bPHY PSD pattern | SP2 link quality: PSD according to PSD mask. | Data signal at SP2 provides data content as specified for MOST50 bPHY PSD pattern. |
| SP2 silent mode | — RL at SP2;<br>— DC offset compensation for SP2 link quality. | Test mode shall ensure:<br>— EBC impedance with AFE impairment detectable;<br>— EBC does not emit data transitions. |
| SP3 silent mode | RL at SP3. | Test mode shall ensure:<br>— BEC impedance with AFE impairment detectable;<br>— no valid data signal present, while stimuli from TDR or VNA may occur. |


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[2] ISO/IEC/IEEE 8802-3:2017, *Information technology — Telecommunications and information exchange between systems — Local and metropolitan area networks — Specific requirements — Part 3: Standard for Ethernet*

[3] ISO/IEC 10731:1994, *Information technology — Open Systems Interconnection — Basic Reference Model — Conventions for the definition of OSI services*

[4] *MOST50 Physical layer stress test tool requirements*[3)]

[5] *MOST50 cPHY tester cable model requirements*[4)]

[6] *MOST FBlock EnhancedTestability*[5)]

[7] *MOST FBlock ExtendedNetworkControl*[6)]

[8] *MOST50 bPHY stress pattern*[7)]

[9] *MOST50 bPHY PSD pattern*[8)]

3) Available at https://standards.iso.org/iso/21806/-1/ed-1/en.

4) Available at https://standards.iso.org/iso/21806/-1/ed-1/en.

5) Available at https://standards.iso.org/iso/21806/-1/ed-1/en.

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