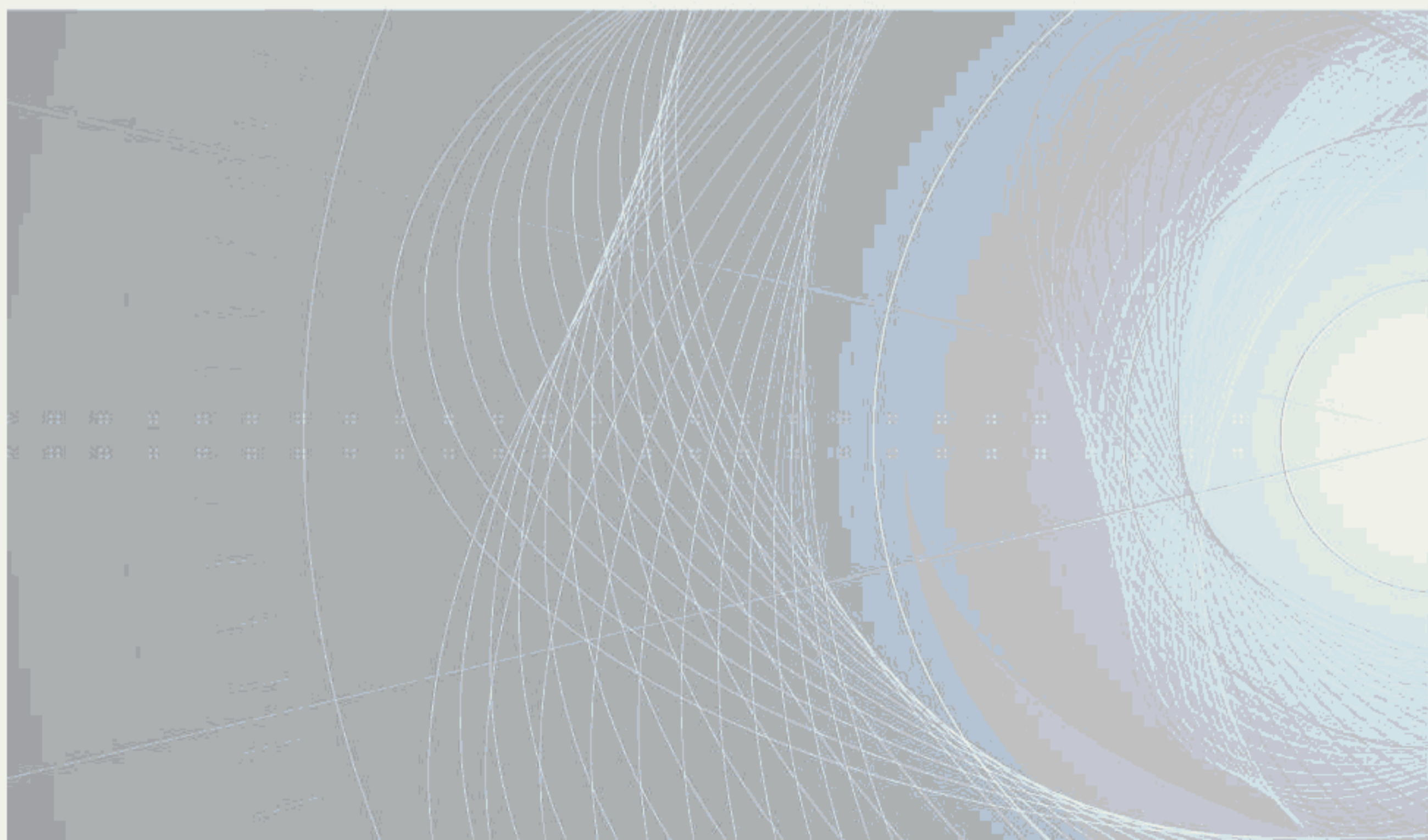


# INTERNATIONAL STANDARD

**Fibre optic active components and devices – Package and interface standards –  
Part 21: Design guidelines of electrical interface of PIC packages using silicon  
fine-pitch ball grid array (S-FBGA) and silicon fine-pitch land grid array  
(S-FLGA)**





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# INTERNATIONAL STANDARD

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## INTERNATIONAL ELECTROTECHNICAL COMMISSION

**FIBRE OPTIC ACTIVE COMPONENTS AND DEVICES –  
PACKAGE AND INTERFACE STANDARDS –****Part 21: Design guidelines of electrical interface of PIC  
packages using silicon fine-pitch ball grid array (S-FBGA)  
and silicon fine-pitch land grid array (S-FLGA)**

## FOREWORD

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IEC 62148-21 has been prepared by subcommittee 86C: Fibre optic systems and active devices, of IEC technical committee 86: Fibre optics. It is an International Standard.

This second edition cancels and replaces the first edition published in 2019. This edition constitutes a technical revision.

This edition includes the following significant technical change with respect to the previous edition: specification of an electric guard band area around the optical terminal area, so as to allow applications with electric signals at higher symbol rates (e.g. 50 Gbaud and 100 Gbaud).

The text of this International Standard is based on the following documents:

CDV	Report on voting
86C/1684/CDV	86C/1710/RVC

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at [www.iec.ch/members\\_experts/refdocs](http://www.iec.ch/members_experts/refdocs). The main document types developed by IEC are described in greater detail at [www.iec.ch/standardsdev/publications](http://www.iec.ch/standardsdev/publications).

A list of all parts in the IEC 62148 series, published under the general title *Fibre optic active components and devices – Package and interface standards*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under [webstore.iec.ch](http://webstore.iec.ch) in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

## **FIBRE OPTIC ACTIVE COMPONENTS AND DEVICES – PACKAGE AND INTERFACE STANDARDS –**

### **Part 21: Design guidelines of electrical interface of PIC packages using silicon fine-pitch ball grid array (S-FBGA) and silicon fine-pitch land grid array (S-FLGA)**

## **1 Scope**

This part of IEC 62148 covers the design guidelines of the electrical interface for photonic integrated circuit (PIC) packages using silicon fine-pitch ball grid array (S-FBGA) and silicon fine-pitch land grid array (S-FLGA). In this document, the electrical interface for the S-FBGA package is informative.

The purpose of this document is to specify adequately the electrical interface of PIC packages composed of optical transmitters and receivers that enable mechanical and electrical interchangeability of PIC packages.

## **2 Normative references**

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60050-731, *International Electrotechnical Vocabulary – Chapter 731: Optical fibre communication* (available at [www.electropedia.org](http://www.electropedia.org))

IEC TR 61931, *Fibre optic – Terminology*

## **3 Terms and definitions**

For the purposes of this document, the terms and definitions given in IEC 60050-731, IEC TR 61931 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

### **3.1**

#### **silicon fine-pitch ball grid array S-FBGA**

device composed of silicon die, dielectric layer(s) on the die, rerouting wires from the die pads to outer balls on the dielectric layer(s), and outer balls with heights more than 0,1 mm

### **3.2**

#### **silicon fine-pitch land grid array S-FLGA**

device composed of silicon die, dielectric layer(s) on the die, rerouting wires from the die pads to outer lands on the dielectric layer(s), and outer lands with heights of 0,1 mm or less

## 4 Terminal position numbering

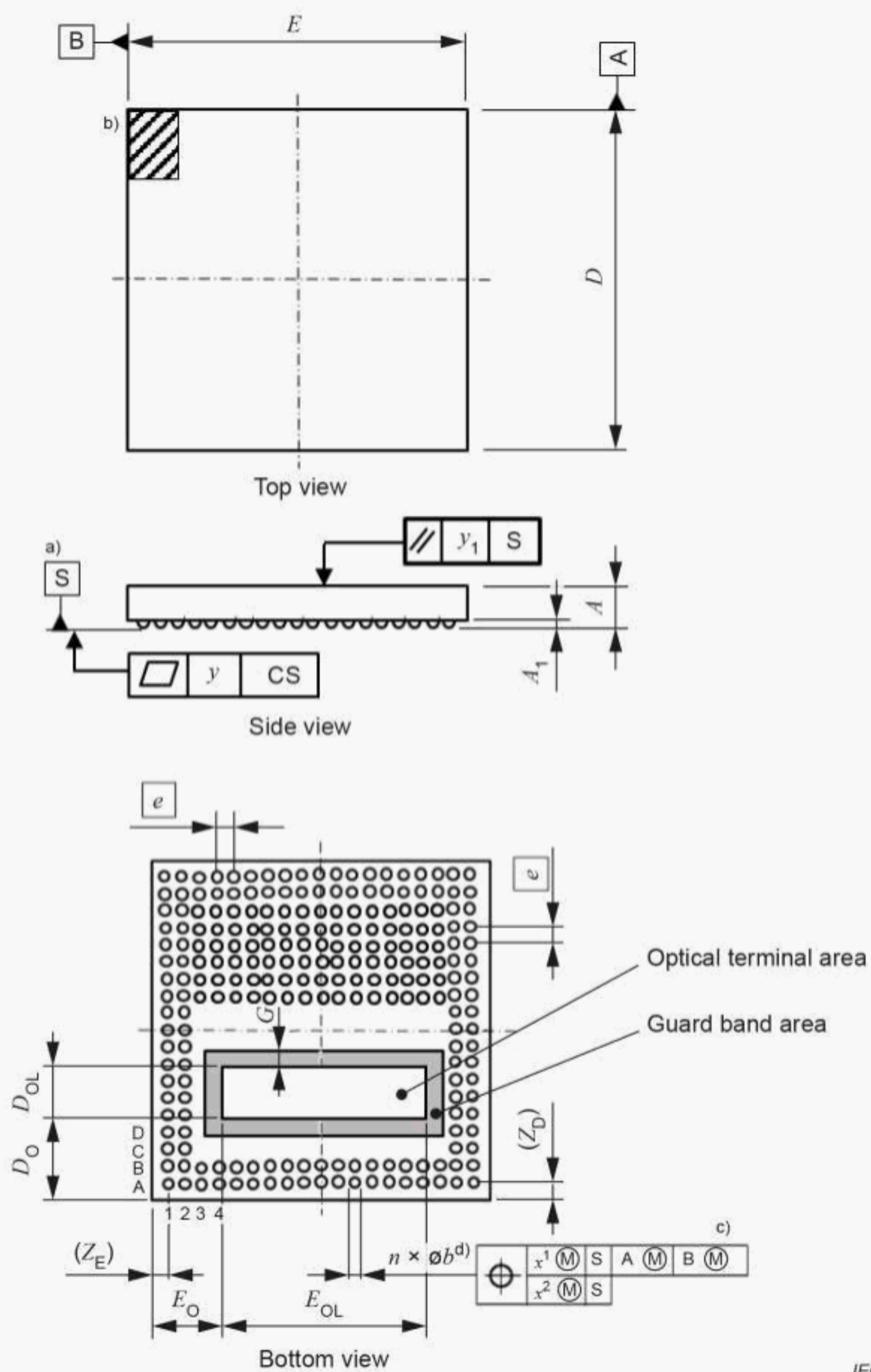
When a package is viewed from the terminal side with the index corner in the bottom left corner position, terminal rows are lettered from bottom to top starting with A, then B, C..., AA, AB, etc.; whereas terminal columns are numbered from left to right starting with 1. Terminal positions are designated by a row-column grid system and shown as alphanumeric identification, for example A1, B1. The letters I, O, Q, S, X and Z shall not be used for naming the terminal rows.

## 5 Code of package nominal dimensions

A code of package nominal dimensions is defined as the combination of package length  $E$  and width  $D$ , which are shown to the second decimal place in millimetres.

## 6 Symbols and drawings

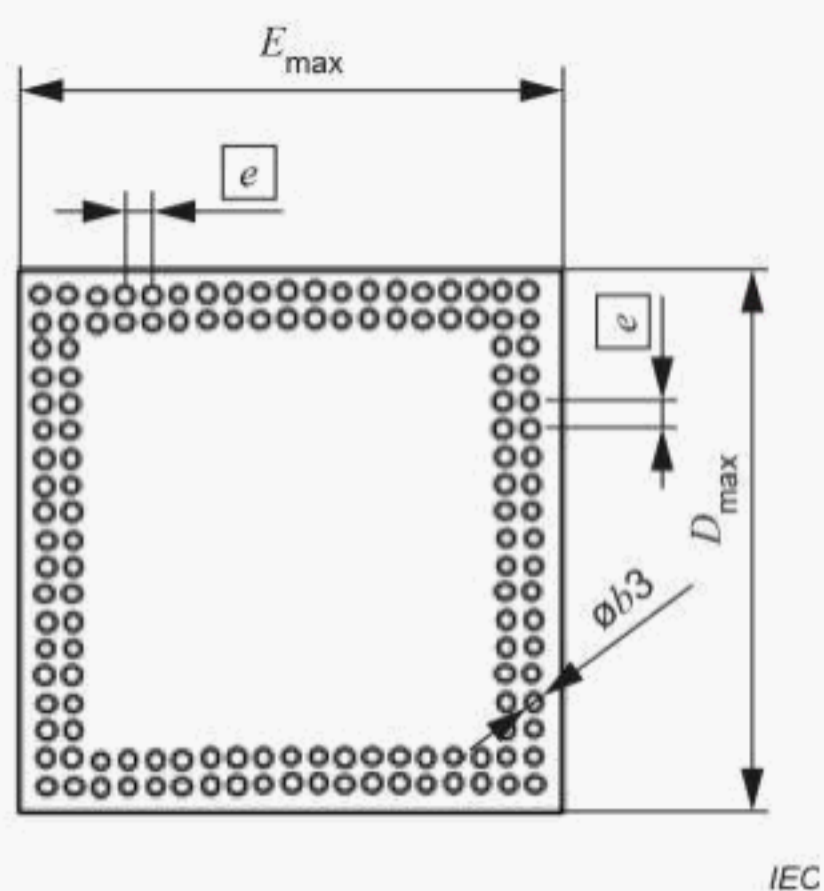
Figure 1 shows the dimensions of the package and the outline of the electrical interface for S-FBGA and S-FLGA. Figure 1 also shows the dimensions of the optical terminal area and its guard band area. The electrical terminal is freely allocated to the terminal positions defined by the cross points of the row-column grid numbers, as long as its position is outside of the optical terminal guard band area. The optical interface shall be designed within the optical terminal area. Figure 2 and Figure 3 indicate the mechanical gauge drawing and its array of electrical terminal existence area. Figure 2 shows the electrical terminal existing area referred to data S, A and B. Figure 3 shows the electrical terminal existing area referred to datum S.



NOTE The letter symbols used in the figure are listed and described in Table 1.

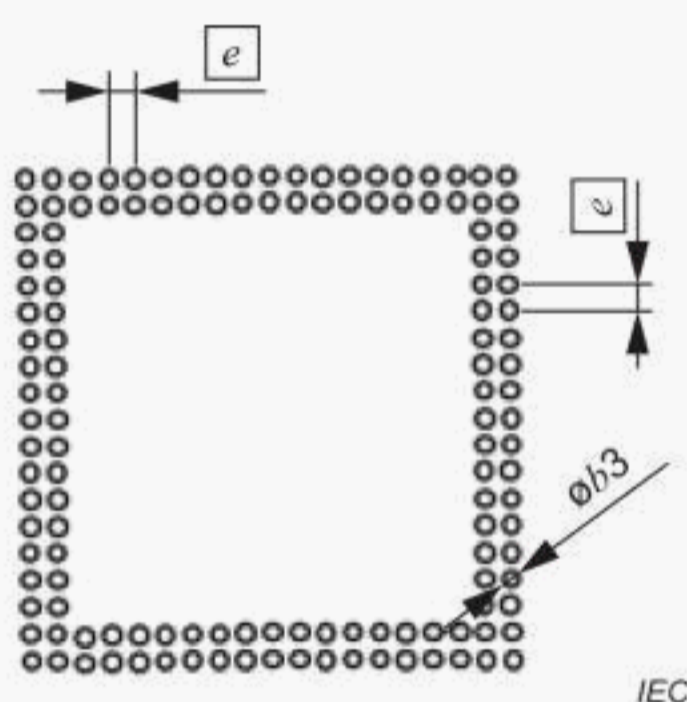
- <sup>a</sup> Datum S is the seating plane on which a package stays.
- <sup>b</sup> The hatched zone is an index-marking area indicating A1 corner.
- <sup>c</sup> True positional tolerances of terminals  $x_1$  and  $x_2$  are applied to all terminals.
- <sup>d</sup> The terminal diameter  $b$  is the maximum diameter of the ball as measured in a plane parallel to the seating plane.

**Figure 1 – S-FBGA and S-FLGA outline**



NOTE The letter symbols used in the figure are listed and described in Table 1.

**Figure 2 – Mechanical gauge drawing**



NOTE The letter symbols used in the figure are listed and described in Table 1.

**Figure 3 – Array of terminal-existence areas**

## 7 Dimensions and tolerances

Table 1 specifies the tolerance of each symbol parameter; Table 2 and Table 3 indicate the options of  $D$ ,  $E$ ,  $MD$  and  $ME$ .

**Table 1 – Dimensions and tolerances**

Term	Symbol	Specification	Recommended value	Notes
Code of package nominal dimensions	$D \times E$	Code of package nominal dimension is defined as the combination of package width $D$ and package length $E$ , which are shown in the second decimal place	-	-
Package width	$D$	Package width is shown in the second decimal place Package width $D_{nom}$ Minimum 0,50 Maximum 10,00 Tolerance $V_D$ $\pm 0,05$		$V_D$ denotes tolerance.
Package length	$E$	Package length is shown in the second decimal place Package length $E_{nom}$ Minimum 0,50 Maximum 10,00 Tolerance $V_E$ $\pm 0,05$		$V_E$ denotes tolerance
Profile height	$A$	When $A$ is $\leq 0,65$ , the tolerance of nominal height is $\pm 0,07$ . When $0,8 \leq A \leq 1,0$ , the tolerance of nominal height is $\pm 0,10$ . $A$ shall not exceed 1,0.		$A$ includes package warpage and tilt allowances.
Stand-off height	$A1$	1) For S-FBGA (informative) $e$ : 0,3 $b_{nom}$ : 0,2 min. 0,1 nom. 0,15 max. 0,2 For low stand-off S-FBGA $A1 \leq 0,20$ 2) For S-FLGA $e$ : 0,25 $A1 \leq 0,10$		
Terminal pitch	$e$	1) For S-FBGA (informative) 0,3 2) For S-FLGA 0,25		
Terminal diameter	$b$	1) For S-FBGA (informative) $e$ : 0,3 min. 0,17 nom. 0,20 max. 0,23 2) For S-FLGA $e$ : 0,25 min. 0,10 nom. 0,13 max. 0,16		
Datum-based positional tolerance of terminals	$x1$	$x1 = 0,08$		

Term	Symbol	Specification	Recommended value	Notes
Relative positional tolerance of terminals	$x_2$	1) For S-FBGA (informative) $e: 0,3 \quad x_2 = 0,03$ 2) For S-FLGA $e: 0,25 \quad x_2 = 0,03$		
Coplanarity	$y$	1) For S-FBGA (informative) $e: 0,3 \quad y = 0,05$ 2) For S-FLGA $e: 0,25 \quad y = 0,05$		
Parallelism of the top surface	$y_1$	$y_1 = 0,08$		
Number of terminals	$n$	$n = M_D \times M_E$ $(M_D - 1) \times M_E$ $M_D \times (M_E - 1)$ $(M_D - 1) \times (M_E - 1)$ $M_E \leq (E - b_{\max} - V_E - x_1 - x_2) / e + 1$ $M_D \leq (D - b_{\max} - V_D - x_1 - x_2) / e + 1$		Numbers of matrices in $M_E$ and $M_D$ are shown in Table 3.
Maximum matrix size in length	$M_E$			
Maximum matrix size in width	$M_D$			
Overhang dimension in width	$Z_D$	$Z_D = [D_{\text{nom}} - (M_D - 1) \times e] / 2$	-	Reference value
Overhang dimension in length	$Z_E$	$Z_E = [E_{\text{nom}} - (M_E - 1) \times e] / 2$	-	Reference value
Datum-defined terminal existence area	$b_3$	$b_3 = b_{\max} + x_1$		
Relative terminal existence area	$b_4$	$b$		
Relative optical terminal area datum position along with width	$D_O$	Design value		
Width of optical terminal area	$D_{OL}$	Design value		
Relative optical terminal area datum position along with length	$E_O$	Design value		
Length of optical terminal area	$E_{OL}$	Design value		
Guard band length	$G$	Design value		

NOTE Dimensions are in millimetres.

**Table 2 – Combination list of  $D$ ,  $E$ ,  $MD$ , and  $ME$  for  $e = 0,30$  mm pitch S-FBGA (informative)**

<b>BGA <math>b_{\max} = 0,23</math></b>		
<b><math>D</math> or <math>E</math></b> mm	<b><math>MD</math> or <math>ME</math></b>	<b><math>MD - 1</math> or <math>ME - 1</math></b>
0,69 to 0,98	2	-
0,99 to 1,28	3	2
1,29 to 1,58	4	3
1,59 to 1,88	5	4
1,89 to 2,18	6	5
2,19 to 2,48	7	6
2,49 to 2,78	8	7
2,79 to 3,08	9	8
3,09 to 3,38	10	9
3,39 to 3,68	11	10
3,69 to 3,98	12	11
3,99 to 4,28	13	12
4,29 to 4,58	14	13
4,59 to 4,88	15	14
4,89 to 5,18	16	15
5,19 to 5,48	17	16
5,49 to 5,78	18	17
5,79 to 6,08	19	18
6,09 to 6,38	20	19
6,39 to 6,68	21	20
6,69 to 6,98	22	21
6,99 to 7,28	23	22
7,29 to 7,58	24	23
7,59 to 7,88	25	24
7,89 to 8,18	26	25
8,19 to 8,48	27	26
8,49 to 8,78	28	27
8,79 to 9,08	29	28
9,09 to 9,38	30	29
9,39 to 9,68	31	30
9,69 to 9,98	32	31
9,99 to 10,28	33	32

**Table 3 – Combination list of  $D$ ,  $E$ ,  $MD$ , and  $ME$  for  $e = 0,25$  mm pitch S-FLGA**

$D$ or $E$ mm	$MD$ or $ME$	$MD - 1$ or $ME - 1$	$D$ or $E$ mm	$MD$ or $ME$	$MD - 1$ or $ME - 1$
0,57 to 0,81	2	-	5,32 to 5,56	21	20
0,82 to 1,06	3	2	5,57 to 5,81	22	21
1,07 to 1,31	4	3	5,82 to 6,06	23	22
1,32 to 1,56	5	4	6,07 to 6,31	24	23
1,57 to 1,81	6	5	6,32 to 6,56	25	24
1,82 to 2,06	7	6	6,57 to 6,81	26	25
2,07 to 2,31	8	7	6,82 to 7,06	27	26
2,32 to 2,56	9	8	7,07 to 7,31	28	27
2,57 to 2,81	10	9	7,32 to 7,56	29	28
2,82 to 3,06	11	10	7,57 to 7,81	30	29
3,07 to 3,31	12	11	7,82 to 8,06	31	30
3,32 to 3,56	13	12	8,07 to 8,31	32	31
3,57 to 3,81	14	13	8,32 to 8,56	33	32
3,82 to 4,06	15	14	8,57 to 8,81	34	33
4,07 to 4,31	16	15	8,82 to 9,06	35	34
4,32 to 4,56	17	16	9,07 to 9,31	36	35
4,57 to 4,81	18	17	9,32 to 9,56	37	36
4,82 to 5,06	19	18	9,57 to 9,81	38	37
5,07 to 5,31	20	19	9,82 to 10,06	39	38

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IEC 60191-6-22, *Mechanical standardization of semiconductor devices – Part 6-22: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for semiconductor packages Silicon Fine-pitch Ball Grid Array and Silicon Fine-pitch Land Grid Array (S-FBGA and S-FLGA)*

IEC 62148-1, *Fibre optic active components and devices – Package and interface standards – Part 1: General and guidance*

IEC 62148-19, *Fibre optic active components and devices – Package and interface standards – Part 19: Photonic chip scale package*

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